Synopsys Introduces New 64-bit ARC Processor IP Delivering Up to 3x Performance Increase for High-End Embedded Applications

DesignWare ARC HS6x Processors Based on New 32/64-bit ARCv3 Instruction Set Architecture Extend Addressable Memory, Scale Up To 12 Cores

MOUNTAIN VIEW, Calif., April 7, 2020 /PRNewswire/ --

Highlights:

- New 64-bit ARCv3 ISA supports 52-bit physical and 64-bit virtual address spaces to enable efficient access to larger memories
- ARC HS5x (32-bit) and HS6x (64-bit) processors scale from one to 12 cores with performance up to 13,750 CoreMarks and 8750 DMIPS per core
- New HS6x processors implement a full 64-bit pipeline and register set and are backwards compatible with existing ARC EM and HS families
- MetaWare Development Toolkit eases development and debugging of highly optimized, high-density code

Synopsys, Inc. (Nasdaq: SNPS) today announced the new DesignWare® ARC® HS5x and HS6x processor IP families for high-performance embedded applications. The 32-bit ARC HS5x and 64-bit HS6x processors, available in single-core and multicore versions, are implementations of a new superscalar ARCv3 Instruction Set Architecture (ISA) and deliver up to 8750 DMIPS per core in 16-nm process technologies under typical conditions, making them the highest performance ARC processors to date.

The multicore versions of the new ARC HS processors include an innovative interconnect fabric that links up to 12 cores and supports interfaces for up to 16 hardware accelerators, all while maintaining coherency among the cores. The processors can be configured for real-time operation or with an advanced memory management unit (MMU) that supports symmetric multiprocessing (SMP) Linux and other high-end operating systems. To accelerate software development, the ARC HS5x and HS6x processors are supported by the ARC MetaWare Development Toolkit that generates highly efficient code. The new ARC HS processors are designed to meet the power, performance, and area requirements of a broad range of high-end embedded applications including solid-state drives (SSDs), automotive control & infotainment, wireless baseband, wireless control, and home networking.

"Designers of high-end embedded applications are under constant pressure to achieve higher performance while addressing larger memory spaces within limited power and area budgets," said Bruce Cheng, Chief Scientist at Starblaze. "The multicore capabilities of Synopsys' new 32-bit ARC HS5x and 64-bit HS6x processors will enable us to scale to new levels of power-performance efficiency, which is not offered by other processors currently on the market."

"The growing complexity of high-end embedded systems such as in networking, storage, and wireless equipment demands greater processor functionality and performance without sacrificing power efficiency," said Mike Demler, senior analyst at The Linley Group. "Synopsys' new ARC HS5x and HS6x CPUs meet those needs, but they also provide the configurability and scalability needed to support future embedded-system requirements as well."

The ARC HS5x and ARC HS6x processors are based on the new ARCv3 ISA that implements a full range

of 32-bit and 64-bit instructions. These processors feature a high-speed 10-stage, dual-issue pipeline that offers increased utilization of functional units with a limited increase in power and area. The HS5x processors feature a 32-bit pipeline that can execute all ARCv3 32-bit instructions, while the HS6x processors feature a full 64-bit pipeline and register file that can execute both 32-bit and 64-bit instructions. In addition, the ARC HS6x supports 64-bit virtual and 52-bit physical address spaces to enable direct addressing of current and future large memories, as well as 128-bit loads and stores for efficient data movement. Multicore versions of both the ARC HS5x and HS6x processors include an advanced high-bandwidth intra-processor interconnect that has been designed to ease development and timing closure with asynchronous clocking and up to 800 GB/s internal aggregate bandwidth. To further simplify physical design and timing closure in multicore configurations, each core can reside in its own power domain and have an asynchronous clock relationship with the other cores. A new 128-bit vector floating point unit supports F16, F32, and F64 operations with a 2-cycle accumulation latency. Like all ARC processors, the HS5x and HS6x processors are highly configurable and implement ARC Processor EXtension (APEX) technology that enables the support of custom instructions to meet the unique performance, power, and area requirements of each target application.

The HS5x and HS6x processors are supported by Synopsys' ARC MetaWare Development Toolkit that includes an advanced C/C++ compiler optimized for the processors' superscalar architecture, a multicore debugger to debug and profile code and a fast instruction set simulator (ISS) for pre-hardware software development. A cycle-accurate simulator is also available for design optimization and verification. Open-source software support for the processors includes the Zephyr real-time operating system, an optimized Linux kernel, the GNU Compiler Collection (GCC), GNU Debugger (GDB), and the associated GNU programming utilities (binutils). Additional hardware and software tools are available from third-party partners, giving developers the flexibility to choose the best and most familiar tools for their design project.

"Embedded applications such as SSDs, wireless control and home networking are becoming increasing complex, requiring significant performance increases within restricted power and area budgets," said John Koeter, senior vice president of Marketing and Strategy for IP at Synopsys. "With the release of the new ARCv3 ISA and launch of ARC HS5x and HS6x processors, designers can address the growing performance demands for their embedded designs today and in the future."

Availability and Resources

The DesignWare ARC HS5x and HS6x processors are scheduled to be available in Q3, 2020. The new processors will include the ARC HS56, HS57D, HS58, HS66, HS68 and multicore versions (HS56MP, HS57DMP, HS58MP, HS66MP, HS68MP) of each.

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes logic libraries, embedded memories, embedded test, analog IP, wired and wireless interface IP, security IP, embedded processors, and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP prototyping kits, IP software development kits and IP subsystems. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enables designers to reduce integration risk and accelerate time-to-market. For more information on DesignWare IP, visit https://www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the

electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

Editorial Contact:
Kelly James
Synopsys, Inc.
650-584-8972
kellyj@synopsys.com

SOURCE Synopsys, Inc.