Synopsys Delivers Industry's First Ethernet 800G Verification IP for Next-Generation Networking and Communications Systems

New Native System Verilog Ethernet VIP Complements Synopsys' 112G High-Speed SerDes PHY IP to Enable High-Performance Cloud Computing Solutions

MOUNTAIN VIEW, Calif., March 23, 2020 /PRNewswire/ -- Synopsys, Inc. (Nasdaq: SNPS) today announced the availability of the industry's first verification IP (VIP) and Universal Verification Methodology (UVM) source code test suite for Ethernet 800G.

As the requirements for increased bandwidth to support video-on-demand, social networking and cloud services continues to rise, Synopsys VC VIP for Ethernet 800G, based on the Ethernet Technology Consortium (ETC) specification, enables system-on-chip (SoC) teams to design next-generation networking chips for data centers with ease of use and fast integration, resulting in accelerated verification closure and time-to-market. The VC VIP is used to verify Synopsys' DesignWare® 56G Ethernet, 112G Ethernet, and 112G USR/XSR PHYs for FinFET processes, which designers can easily integrate into 800G SoCs to meet their long reach and short reach interface requirements.

The ETC standard provides specifications for an 800G implementation based on 8 lane x 100 Gb/s technology, enabling adopters to deploy advanced high bandwidth interoperable Ethernet technologies.

"Our 800 Gigabit Ethernet Core will help our customers create flexible system solutions for 800 Gigabit Ethernet applications," said Francois Balay, president of MorethanIP. "Being first in the industry, Synopsys VIP, source code test suite, and DesignWare IP for Ethernet 800G strengthens the ecosystem and facilitates early adoption of the technology and fast development of high-speed networking applications."

Synopsys VC VIP for Ethernet uses a native System Verilog UVM architecture, protocol-aware debug and source code test suites. Synopsys VC VIP can switch speed configurations dynamically at run time and includes an extensive and customizable set of frame generation and error injection capabilities. In addition, source code UNH-IOL test suites are available for key Ethernet features and clauses, allowing teams to quickly jumpstart their own custom testing and accelerate verification closure.

"As a leader in verification IP, Synopsys continues to stay in the forefront to deliver another industry-first VIP solution for Ethernet 800G," said Vikas Gautam, vice president of engineering of VIP R&D for the Synopsys Verification Group. "To achieve these industry firsts, Synopsys continues to innovate and provide support for the latest specifications, enabling leading IP design and SoC companies to quickly verify their products and accelerate time to market."

Availability

Synopsys VC VIP and source code test suite for Ethernet 800G are both available today as early access standalone products. The DesignWare 56G and 112G Ethernet PHYs are available now. The silicon design kit for the DesignWare USR/XSR PHY IP in 7nm FinFET process is available now.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

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