Synopsys Unveils RTL Architect To Accelerate Design Closure

Unique RTL Tuning Environment Reduces Physical Design Iterations

MOUNTAIN VIEW, Calif., March 16, 2020 /PRNewswire/ --

Highlights:

- The RTL Architect product represents the industry's first physically aware RTL analysis, optimization, and signoff system built on a fast, multi-dimensional prediction engine for superior RTL handoff
- The unified Fusion data model delivers unprecedented capacity and scalability for enabling full-chip hierarchical RTL design flows
- The new product leverages Synopsys' world-class implementation and golden signoff solutions to deliver results that correlate-by-construction
- Synopsys and Arm are collaborating on RTL Architect to accelerate the development of next-generation cores

Synopsys, Inc. (Nasdaq: SNPS) today announced the immediate availability of RTL Architect™, an innovative product that signifies a shift-left for RTL design closure. Synopsys RTL Architect is the industry's first physically aware RTL design system, which reduces the SoC implementation cycle in half and delivers superior quality-of-results (QoR).

RTL teams are increasingly faced with the challenges of rapidly exploring domain-specific RTL architectures to achieve significant power, performance and area (PPA) gains to meet the requirements of new market verticals like artificial intelligence and automotive applications. Existing point tool solutions for estimating RTL quality are severely limited due to poor accuracy to downstream implementation. These early design cycle inaccuracies cause downstream implementation tools to compensate, often having to go back and make RTL changes to meet the PPA goals. RTL Architect addresses these challenges utilizing a rapid multi-objective prediction engine derived from the Synopsys Fusion Design Platform implementation environment to predict PPA of downstream implementation accurately. RTL Architect enables RTL designers to pinpoint bottlenecks in their source code to improve RTL quality.

"Renesas is designing complex state-of-the-art automotive system on chips (SoCs), which require architecture tuning to drive the highest QoR to differentiate ourselves in our target markets," said Hideyuki Okabe, Director, Digital Design Technology Department, Shared R&D EDA Division, Renesas Electronics Corporation. "Synopsys' RTL Architect will enable us to quickly explore and validate various architectures at the RTL stage and identify the best one without having to worry about late-stage surprises."

"Our collaboration with Synopsys on the RTL Architect product is the next step in helping to accelerate our RTL development cycle for the next-generation of Arm®-based processor cores," said Jeff Kehl, vice president of CPU engineering, Central Engineering Group, Arm. "RTL Architect technologies in our advanced core development design methodology will enable Arm to develop better CPUs that allow our mutual customers to meet the power and performance requirements for a number of new markets."

The RTL Architect system is built on a unified data model that provides multi-billion gate capacity and comprehensive hierarchical design capabilities to accommodate the growing design and block sizes at advanced process nodes. It directly leverages Synopsys' world-class implementation and golden signoff solutions to deliver results that are accurate early in the design cycle and correlate-by-construction.

RTL Architect uses a fast, multi-dimensional implementation prediction engine that enables RTL designers to predict the power, performance, area, and congestion impact of their RTL changes. Synopsys' PrimePower golden signoff power analysis engine is directly integrated for accurate RTL power estimation and optimization for energy-efficient designs. RTL Architect provides a unified workflow environment for simplified ease-of-use and seamless analysis of key PPA quality metrics. For existing users of PrimePower at the gate-level, PrimePower RTL power estimation is also available, enabling a consistent RTL to signoff power analysis flow.

"As we move to smaller technology nodes, it is critical to enable fast RTL tuning iterations and rapid architecture exploration for driving best design PPA. Addressing these challenges early in the design cycle and crafting top-quality RTL are essential for achieving the best QoR and fastest time to results," said Shankar Krishnamoorthy, senior vice president of design implementation for the Design Group at Synopsys. "RTL Architect has been devised to solve the growing demands of the design community, so designers are able to confidently hand off superior RTL for a convergent design flow and best PPA."

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

Editorial Contact:
Simone Souza
Synopsys, Inc.
650-584-6454
simone@synopsys.com

SOURCE Synopsys, Inc.