Samsung Adopts Synopsys' Machine Learning-Driven IC Compiler II for its Next-Generation 5nm Mobile SoC Design

Recent Advances in Machine Learning (ML) Technologies Extend Synopsys' QoR Leadership

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Highlights:

- ML-driven implementation in IC Compiler II and Fusion Compiler enables Samsung to achieve up to five percent higher frequency and five percent lower power
- Predictive ML technologies accelerate turn-around-time (TAT), allowing Samsung to meet aggressive design schedules
- Samsung has deployed ML technologies in imminent tape-out of its next-generation mobile SoC

Synopsys, Inc. (Nasdaq: SNPS) today announced that Samsung has adopted the industry-leading IC Compiler™ II place-and-route solution, part of the Synopsys Fusion Design Platform™, for its next-generation 5nm mobile system-on-chip (SoC) production design. In order to meet the aggressive design goals of this complex SoC, Samsung employed IC Compiler II's cutting-edge machine learning technologies resulting in significant QoR and productivity boosts of up to five percent higher frequency, five percent lower leakage power and faster TAT. The rapid development of Samsung's high-volume mobile SoC marks an important milestone as the first production design at Samsung to leverage IC Compiler II's ML-implementation technologies.

"We constantly look for ground-breaking technologies from EDA vendors to enable pushing the power, performance and area (PPA) envelope for our next-generation products," said Youngmin Shin, vice president of System LSI Design Technology at Samsung Electronics. "Machine learning-driven chip design represents a paradigm shift which delivers a significant QoR and productivity leap required to tackle the mounting challenges of smaller geometries. We are extremely impressed with Synopsys for making the ML vision a reality in IC Compiler II and delivering exceptional QoR results."

ML offers opportunities to enable self-optimizing design tools that can continuously learn and improve in customer environments, giving Synopsys a new arsenal of solutions for today's demanding semiconductor market. ML-driven capabilities in Synopsys' IC Compiler II and Fusion Compiler™ implementation solution capture design behavior at multiple stages of design evolution, offering upstream engines faster and accurate visibility into complex downstream effects - allowing designers to achieve new levels of productivity and QoR. Today's announcement is part of a multi-year initiative and strategic investment in ML technology at Synopsys' Design Group, aimed at enabling an orchestrated, self-optimizing design environment with ML, everywhere.

"Synopsys' investment into machine learning-driven implementation and signoff has opened up new avenues to further extend our PPA leadership with unsurpassed design QoR and TTR," said Sanjay Bali, vice president of marketing, Design Group at Synopsys. "Through deep collaborations with our technology-leading partners like Samsung, we are able to develop and deploy machine-learning technologies to help customers realize their ultra-complex chip designs."

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

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