Synopsys' Fusion Compiler Adopted by AMD

Synopsys and AMD Collaborate to Optimize Synopsys' Fusion Compiler for Servers Powered by AMD EPYC Processors

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Highlights:

- AMD deploys Synopsys' Fusion Compiler RTL-to-GDSII product for the development of its next-generation processor products
- Unique, single-data-model architecture and unified, full-flow optimization engines deliver superior performance, power and area metrics

Synopsys, Inc. (Nasdaq: SNPS) today announced that AMD is deploying Synopsys' Fusion Compiler™ RTL-to-GDSII product for its full-flow, digital-design implementation. Based on an evaluation process, the Fusion Compiler product delivered industry-leading performance, power and area (PPA) metrics. This work has additionally resulted in an expanded collaboration between Synopsys and AMD to optimize Synopsys applications on AMD EPYC™ processors, targeted to deliver marked runtime acceleration benefits when deploying the Fusion Compiler RTL-to-GDSII product across servers powered by AMD EPYC processors. These advancements will be made available to all users in upcoming service packs.

"At AMD, we are committed to exceeding customer expectations by continually expanding our leadership position in high-performance computing," said Mark Papermaster, Chief Technology Officer and Executive Vice President, Technology and Engineering at AMD. "Based on our evaluation results, Synopsys' Fusion Compiler helped us meet our performance and time-to-market goals for our latest products. As a result, we plan to use Fusion Compiler for the development of our next-generation products."

"Synopsys' Fusion Compiler product is the successful result of a multi-year investment in a vision to build highly differentiated and transformative products for an increasingly demanding industry," said Sassine Ghazi, general manager, Design Group at Synopsys. "It is very satisfying to see dozens of customers across the industry rapidly realize the benefits of the new product and extract previously untapped value in their digital designs. We are excited to work with market leaders like AMD who are benefiting from these leaps in innovation to deliver exciting products to their existing markets and creating the path to new ones."

The Fusion Compiler product is uniquely architected to enable design teams to achieve the optimal levels of power, performance, and area (PPA) in the most convergent manner to ensure the fastest and most predictable time-to-results (TTR). Built using a single, highly-scalable data model, and based around an analysis backbone that leverages technology from the industry's golden-signoff analysis tools, Fusion Compiler guarantees that these critical PPA metrics are optimized efficiently and effectively throughout the full RTL-to-GDSII design flow. Fusion Compiler delivers best-in-class PPA through a highly-leveraged optimization framework, resulting in a fully-unified physical synthesis and optimization methodology where industry-leading technologies can be deployed at any point throughout the flow for maximum effect. This groundbreaking approach delivers better timing, better total power, and improved area density compared to using a traditional combination of front- and back-end tools. Fusion Compiler offers Simply Better PPA™.

About Fusion Technology™

Synopsys' breakthrough Fusion Technology™ transforms the RTL-to-GDSII design flow with the fusion of best-in-class optimization and industry-golden signoff tools, enabling designers to accelerate the delivery of their next-generation designs with the industry-best full-flow quality of results (QoR) and the fastest TTR. It redefines conventional EDA tool boundaries across synthesis, place-and-route, and signoff, sharing engines across the industry's premier digital design tools, and using a unique, single data model for both logical and physical representation. Fusion Technology enables one DNA backbone across the Synopsys Design Platform that includes IC Compiler™ II place-and-route, Design Compiler® Graphical synthesis, PrimeTime® signoff, StarRC™ extraction, IC Validator physical verification, DFTMAX™ test, TetraMAX® II automatic test pattern generation (ATPG), SpyGlass® DFT ADV RTL testability analysis, and Formality® equivalence checking. It provides Design Fusion, ECO Fusion, Signoff Fusion, and Test Fusion, resulting in the most predictable RTL-to-GDSII flow with the fewest iterations, as well as unsurpassed design frequency, power, and area.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the

electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

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