Synopsys VC LP for Low Power Signoff Verification Delivers Up to 5X Runtime Gain at Samsung

Signoff Abstract Model Flow for Hierarchical Verification Delivers Higher Performance and Capacity with No Loss in Quality of Results or Debug Visibility

MOUNTAIN VIEW, Calif., Nov. 7, 2019 /PRNewswire/ -- Synopsys, Inc. (Nasdaq: SNPS) today announced that Samsung, a global leader in enterprise mobility and information technology, has adopted the Synopsys VC LP™ solution, part of the Verification Continuum™ Platform, for low-power signoff and static verification to minimize costly design iterations for large-scale, complex system-on-chip (SoC) designs. The recently expanded VC LP solution includes the Signoff Abstract Model (SAM) based methodology, which enabled Samsung to achieve up to 5X performance gains and up to 6X less memory footprint with the same quality of results (QoR) and debug visibility compared to flat run methods for low-power signoff.

"Maintaining performance and quality of results during low-power verification signoff is a must-have requirement," said Jung Yun Choi, vice president of Foundry Design Technology Team at Samsung Electronics. "Using the Signoff Abstract Model flow in the VC LP solution enables us to accelerate static low-power verification by 5X, and ensures high-quality QoR and signoff for our ASIC designs. With minimal changes to existing environment configuration, the hierarchical flow can be seamlessly adopted over several designs, effectively supporting the expedition of high-quality ASIC delivery."

The SAM flow enables library cells, hierarchical instances, and net connections that are not essential for top-level verification to be removed, resulting in a new abstracted block-level model. The abstract model methodology decides the amount of logic to retain in the block to ensure highest performance and QoR.

In addition to the SAM flow, the VC LP solution also includes the newly introduced machine learning-enabled analysis technology for improved QoR and better debugability. This technique helps to significantly reduce the overall turnaround time for verification signoff to ensure that subtle bugs do not escape into silicon.

"The use of a signoff abstract model-based flow and machine learning technology is crucial for customers to save critical man hours and avoid iterative analysis during ASIC verification," said Sridhar Seshadri, vice president of engineering for the Verification Group at Synopsys. "Our VC LP hierarchical-based SAM flow provides Samsung with the same level of confidence as flat runs on large SoC designs, which has been a game-changer for achieving the highest design quality."

Synopsys hosted two webinars to introduce the hierarchical flow and machine learning-enabled solutions in VC LP. A replay of these webinars can be accessed here: https://readytalk.webcasts.com/starthere.jsp?ei=1229181&tp_key=a02c90b91a&sti=web
https://readytalk.webcasts.com/starthere.jsp?ei=1252774&tp_key=8a39d4e204&sti=web

Availability

Synopsys VC LP is available now.

Additional Resources

For more information on VP LP, please visit: https://www.synopsys.com/verification/static-and-formal-verification/vc-lp.html

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP, and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

Editorial Contact:
James Watts
Synopsys, Inc.
650-584-1625
jwatts@synopsys.com

SOURCE Synopsys, Inc.