Synopsys Accelerates Cloud Computing SoC Designs with New Die-to-Die PHY IP in Advanced 7nm FinFET Process

DesignWare Die-to-Die PHY Enables Ultra- and Extra-Short Reach Connectivity in Large, Multi-Chip Module Designs

MOUNTAIN VIEW, Calif., Oct. 29, 2019 /PRNewswire/ -- **Highlights:**

- Ultra-low power DesignWare Die-to-Die PHY IP delivers less than 1pJ/bit for optimal energy efficiency in hyperscale data centers
- Compact analog front-end enables reliable links up to 50 millimeters for large multi-chip module designs
- Flexible architecture enables partitioning of the core logic across multiple dies with extremely low-latency and bit error rate
- Combined with the DesignWare 112G/56G Ethernet, HBM2/2E, DDR5/4, and PCI Express 5.0 IP, Synopsys provides a comprehensive solution for high-performance computing and networking SoCs

Synopsys, Inc. (Nasdaq: SNPS) today announced its DesignWare® Die-to-Die PHY IP for ultra- and extra-short reach connectivity in multi-chip modules (MCM) for hyperscale data center, AI, and networking designs. The DesignWare Die-to-Die PHY IP supports NRZ and PAM-4 signaling from 2.5G to 112G data rates, delivering maximum throughput per die edge for large MCM designs. To improve SoC yield, the Die-to-Die PHY allows for partitioning of large dies into smaller dies while offering trade-offs for power, bandwidth per beachfront, latency, and reach. The DesignWare Die-to-Die PHY is the latest addition to Synopsys' comprehensive cloud computing IP solution consisting of silicon-proven 112G/56G Ethernet HBM2/2E, DDR5/4, and PCI Express 5.0 controller, PHY, and verification IP.

Synopsys provides designers with a comprehensive routing feasibility analysis, packages substrate guidelines, signal and power integrity models, and crosstalk analysis for fast integration of the DesignWare Die-to-Die PHY into SoCs. The half-duplex transmitter and receiver in a X16 lane configuration delivers 1.8 terabit-per-second per millimeter unidirectional bandwidth for high throughput die-to-die connectivity. To meet the power requirements of SoCs in advanced FinFET processes, the Die-to-Die PHY delivers less than one picojoule per bit (pJ/bit) for ultra-low-power die-to-die and die-to-optical engine connectivity. The DesignWare Die-to-Die PHY IP is compliant with the OIF CEI-112G and CEI-56G standards for ultra-short reach (USR) and extra-short reach (XSR) links.

"Advanced SoCs for high-end data center and networking applications are reaching maximum reticle size limits, requiring designers to partition the SoC into smaller modular dies," said John Koeter, vice president of marketing for IP at Synopsys. "The DesignWare Die-to-Die PHY IP with leading power, performance, and area is enabling our customers to meet their short reach connectivity requirements in designs for the most advanced FinFET processes and deliver differentiated products to the market quickly."

Availability

The silicon design kit for the DesignWare Die-to-Die PHY IP in 7nm FinFET process is available now.

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes logic libraries, embedded memories, embedded test, analog IP, wired and wireless interface IP, security IP, embedded processors, and subsystems. To accelerate prototyping, software development, and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP prototyping kits, IP software development kits, and IP subsystems. Synopsys' extensive investment in IP quality, comprehensive technical support, and robust IP development methodology enable designers to reduce integration risk and accelerate time-to-market. For more information on DesignWare IP, visit https://www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

Forward-Looking Statements

This press release contains forward-looking statements within the meaning of Section 21E of the Securities Exchange Act of 1934, including statements regarding the expected release and benefits of DesignWare Interface and Foundation IP for TSMC's N5P process including for USB, DisplayPort, DDR, LPDDR, HBM, PCI Express, Ethernet, MIPI, and HDMI. Any statements that are not statements of historical fact may be deemed to be forward-looking statements. These statements involve known and unknown risks, uncertainties and other factors that could cause actual results, time frames, or achievements to differ materially from those expressed or implied in the forward-looking statements. Such risks and uncertainties include, among others, product timeline and development schedules, or interoperability, performance, and power issues. Other risks and uncertainties that may apply are set forth in the "Risk Factors" section of Synopsys' most recently filed Quarterly Report on Form 10-Q. Synopsys undertakes no obligation to update publicly any forward-looking statements, or to update the reasons actual results could differ materially from those anticipated in these forward-looking statements, even if new information becomes available in the future.

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