Astera Labs Accelerates PCI Express 5.0 System Deployment in Collaboration with Intel and Synopsys

Astera Labs Delivers Industry's First Commercially Available PCIe 5.0 Retimer SoC

MOUNTAIN VIEW, Calif., Oct 23, 2019 **Highlights:**

- Astera Labs' Aries Smart Retimer is the industry's first 32GT/s retimer SoC designed to the PCIe 5.0 specification. It doubles the signal reach and achieves plug-and-play interoperation without compromising interconnect topologies even at 32 GT/s speeds.
- Astera Labs achieved first-pass silicon success for its retimer SoC using Synopsys' DesignWare IP and Verification IP solutions for PCIe 5.0. The DesignWare IP has been adopted by more than a dozen leading semiconductor companies across all key market segments and has demonstrated proven interoperability with a range of products in the industry.
- The end-to-end system demonstration is a key milestone in the companies' ongoing collaboration to advance the PCIe 5.0 ecosystem.
- Astera Labs, in collaboration with Synopsys and Intel, will demonstrate system-level interoperability of an end-to-end PCIe 5.0 solution during PCI-SIG Developers Conference in Taipei, October 28-29.

Astera Labs Inc., in collaboration with Synopsys, Inc. (Nasdaq: SNPS), and Intel (Nasdaq: INTC), today announced an industry-first demonstration of a complete PCI Express® (PCIe®) 5.0 system, delivering 32 GT/s speeds for next-generation server workloads. The end-to-end solution showcases system-level multi-vendor interoperability between Intel's PCIe 5.0 test chip, Synopsys' silicon-proven DesignWare® Controller and PHY IP for PCIe 5.0, and Astera Labs' industry-first Smart Retimer SoC for PCIe 5.0. The companies will demonstrate the solution at the PCI-SIG Developers Conference in Taipei, October 28-29.

"We're excited to collaborate with Synopsys and Intel to prove to the industry that we are ready for PCIe 5.0 customers and we are actively sampling our retimer SoC now," said Jitendra Mohan, chief executive officer, Astera Labs. "We've delivered the world's first PCIe 5.0 Smart Retimer that provides backwards compatibility, enabling developers to future-proof their systems by leveraging the solution for PCIe 4.0 now and having a pin-compatible solution for PCIe 5.0 when systems are available in 2020. Collaborating with Synopsys and Intel helped accelerate our development process."

"Synopsys, Astera Labs, and Intel are collaborating to help the PCI Express ecosystem to meet their advanced requirements for networking, storage, and machine learning applications that require extremely high-speed interfaces," said John Koeter, vice president of marketing for IP at Synopsys. "By providing a complete IP solution for PCI Express 5.0, Synopsys enables companies like Astera Labs to get an early start on their designs and benefit from Synopsys' proven expertise in PCI Express to achieve first-pass silicon success for their SoCs."

"PCIe 5.0 technology adoption is crucial as the industry adds accelerated, heterogenous computing architectures and workload-optimized platforms to support the next generation of data-centric platform," said Jim Pappas, director of Technology Initiatives at Intel. "Intel is a staunch proponent of PCIe 5.0 architecture and we are racing to deliver robust solutions that deliver faster speeds and lower latency to meet data centric workload requirements. We are pleased to collaborate with Astera Labs and Synopsys on pioneering this new ecosystem."

Demonstration at PCI-SIG Developers Conference in Taipei
The joint PCIe 5.0 demonstration will be showcased in the Synopsys Booth at PCI-SIG DevCon Taipei, October 28-29 at the Taipei Marriott Hotel.

About DesignWare IP
Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes logic libraries, embedded memories, embedded test, analog IP, wired and wireless interface IP, security IP, embedded processors, and subsystems. To accelerate prototyping, software development, and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP prototyping kits, IP software development kits, and IP subsystems. Synopsys' extensive investment in IP quality, comprehensive technical support, and robust IP development methodology enable designers to reduce integration risk and accelerate time-to-market. For more information on DesignWare IP, visit https://www.synopsys.com/designware.

About Synopsys
Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software

company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

About Astera Labs
Astera Labs Inc., a fabless semiconductor company headquartered in Silicon Valley, is a leader in purpose-built connectivity solutions for data-centric systems. Its product portfolio includes system-aware semiconductor integrated circuits, boards and services to enable robust PCI Express® connectivity. Partnering with leading processor vendors, cloud service providers, seasoned investors and world-class manufacturing companies, Astera Labs is helping customers remove performance bottlenecks in compute-intensive workloads. For more information, visit www.AsteraLabs.com.

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