Synopsys and TSMC Collaborate to Develop Portfolio of DesignWare IP for TSMC 5nm FinFET Plus (N5P) Process

Interface and Foundation IP Enables Next Wave of Low-Power Mobile and High-Performance Cloud Computing SoCs on TSMC's N5P Process

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Highlights:

- DesignWare PHY IP in development on TSMC's N5P process includes USB, DisplayPort, DDR, LPDDR, HBM, PCI Express, Ethernet, MIPI, and HDMI
- DesignWare Foundation IP on TSMC's N5P process encompasses high-speed, area-optimized, and low-power embedded memories, logic libraries, and one-time programmable non-volatile memory
- STAR Memory System™ with new algorithms targeting 5nm FinFET-based transistor defects allow efficient test, repair, and diagnostics of embedded memories

Synopsys, Inc. (Nasdaq: SNPS) today announced a collaboration with TSMC to develop a broad portfolio of DesignWare® interface IP, logic libraries, embedded memories, and one-time programmable (OTP) non-volatile memory (NVM) IP on TSMC's 5-nanometer (nm) FinFET Plus (N5P) Process. The DesignWare IP solutions for TSMC's N5 process will enable designers to achieve aggressive performance, density, and power targets for their mobile and cloud computing designs. This collaboration reinforces the longstanding relationship between the two companies to provide designers with the high-quality IP needed to lower risk, differentiate their system-on-chips (SoCs), and accelerate their time-to-market.

"For nearly two decades, TSMC has been collaborating closely with Synopsys to help our mutual customers accelerate their time to volume by providing a broad range of proven DesignWare IP on TSMC's most advanced processes," said Suk Lee, senior director of the Design Infrastructure Management Division at TSMC. "We're pleased with the results of our collaboration in enabling designers to achieve an acceleration on their advanced mobile and cloud computing SoCs while gaining the full performance and power benefits of TSMC's newest and industry-leading process technology."

"As the leading provider of interface IP, Synopsys continues to make significant investments in developing high-quality IP on the latest process technologies, so designers can gain the performance, power, and area advantages that help differentiate their SoCs," said John Koeter, vice president of marketing for IP at Synopsys. "Our collaboration with TSMC on the development of Synopsys' DesignWare IP for the N5P process will enable designers to achieve their aggressive design goals and accelerate their project schedules in today's fast-moving markets."

Availability

The DesignWare Interface and Foundation IP for TSMC's N5P process are scheduled to be available starting in Q4 of 2019.

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes logic libraries, embedded memories, embedded test, analog IP, wired and wireless interface IP, security IP, embedded processors, and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP prototyping kits, IP software development kits, and IP subsystems. Synopsys' extensive investment in IP quality, comprehensive technical support, and robust IP development methodology enable designers to reduce integration risk and accelerate time-to-market. For more information on DesignWare IP, visit https://www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

Forward-Looking Statements

This press release contains forward-looking statements within the meaning of Section 21E of the Securities Exchange Act of 1934, including statements regarding the expected release and benefits of DesignWare Interface and Foundation IP for TSMC's N5P process including for USB, DisplayPort, DDR, LPDDR, HBM, PCI Express, Ethernet, MIPI, and HDMI. Any statements that are not statements of historical fact may be deemed to be forward-looking statements. These statements involve known and unknown risks, uncertainties and other factors that could cause actual results, time frames or achievements to differ materially from those expressed or implied in the forward-looking statements. Such risks and uncertainties include, among others, product timeline and development schedules, or interoperability, performance, and power issues. Other risks and uncertainties that may apply are set forth in the "Risk Factors" section of Synopsys' most recently filed Quarterly Report on Form 10-Q. Synopsys undertakes no obligation to update publicly any forward-looking statements, or to update the reasons actual results could differ materially from those anticipated in these forward-looking statements, even if new information becomes available in the future.

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