Synopsys and TSMC Collaborate for Certification on 5nm Process Technologies to Address Next-generation HPC, Mobile Design Requirements

Enhancements in Design and Verification Tools Target Gains in Performance and Ultra-low Power

MOUNTAIN VIEW, Calif., Sep 26, 2019 /PRNewswire/ --

Highlights:

- Tools certified for the latest version of TSMC's N5/N5P DRM and SPICE model
- Synopsys power optimization enabled to support ultra-low power requirement of mobile devices
- Implementation vs. signoff correlation, certified for timing and extraction, reduces time-to-market
- Collaboration also extended to certification on TSMC's N6 process technology for early customer engagement

Synopsys, Inc. (Nasdaq: SNPS) today announced it has achieved certification for dozens of new, innovative features to the Synopsys Digital and Custom Design Platforms on TSMC's most advanced 5nm process technology, required for high-performance computing (HPC) and mobile chip designs. In addition to certification of HPC and mobile design flows, Synopsys has also achieved the certification for its design tools on TSMC's industry-leading N5P and N6 process technologies, enabling early customer design work.

"Our close collaboration with Synopsys ensures a well-established design flow to help customers address the requirements on increasing complexities for their HPC and mobile designs and achieve their success of silicon innovations on 5-nanometer processes," said Suk Lee, senior director of the Design Infrastructure Management Division at TSMC. "Partnering with our ecosystem, TSMC continues to push the leading edge for enablement of HPC and mobile design solutions on TSMC's most advanced 5-nanometer processes."

Enhancements to multiple design tools in the HPC and mobile design flows enable designers to maximize the advantages of TSMC's 5nm processes in logic density, performance, and power over previous-generation process nodes. Starting with floorplanning and placement, new features in Synopsys Design Compiler® Graphical synthesis and IC Compiler™ II place-and-route were created to handle new 5nm placement rules for spacing, abutment, and boundary cell insertion. For the ultra-low power needs of mobile devices, an increasing variety and usage of low-leakage cells is needed. Therefore, enhancements were also made in IC Compiler II to handle the increased complexity of legalizing low-leakage cell placement. As part of the HPC and mobile design flow platform certification, results from Synopsys' StarRC™ and PrimeTime® signoff solutions were rigorously compared to implementation results to successfully achieve design flow correlation targets that will improve design convergence and shorten overall time-to-market.

"Rapid innovations in the HPC and mobile markets require SoC teams to explore how best to leverage 5-nanometer process technologies, and it is imperative for us to enable our customers to meet their design and time-to-market requirements," said Michael Sanie, vice president of marketing and strategy of the Design Group at Synopsys. "This latest collaboration with TSMC that will better enable HPC and mobile design customers is one part of a continuous endeavor to provide best-in-class solutions for optimized performance, power, and logic density, and help them get to market on time."

Key products and features of the Synopsys design platforms included in these collaborations include:

- **IC Compiler II place-and-route:** Fully automated, full-color routing and extraction support coupled with extended via-pillar automation. Deployment of next-generation placement and legalization technologies, including advanced pin-access modeling to support aggressive cell footprint shrinks and enable higher design utilizations.
- **PrimeTime timing signoff:** Advanced variation modeling for low voltages, and enhanced ECO technologies with support for new physical design rules.
- **PrimePower power signoff:** Advanced, physically-aware power modeling to accurately analyze leakage effects of ultra-high-density standard cell designs.
- **StarRC extraction signoff:** Advanced modeling to handle the complexity of 5nm devices, as well as a common technology file for parasitic extraction consistency from synthesis to place-and-route to signoff.
- **IC Validator physical signoff:** Qualified DRC, LVS, and fill runsets developed natively. DRC runset released at the same time that TSMC released the design rules.
- **HSPICE®, CustomSim™, and FineSim® simulation solutions:** Accurate FinFET device modeling with Monte Carlo feature support and circuit simulation of analog, logic, high-frequency, and SRAM designs.
- **CustomSim reliability analysis:** Self-heat-aware dynamic transistor-level IR/EM analysis certified for

5nm EM rules.

- **Custom Compiler™ custom design:** Support for new 5nm design rules, coloring flow, poly track regions, and new MEOL connectivity requirements.
- **NanoTime custom timing signoff:** Runtime optimization for 5nm devices, POCV analysis for FinFET stacks, and enhanced signal integrity analysis for custom logic and embedded SRAMs.
- **ESP-CV custom functional verification:** Transistor-level symbolic equivalence checking for SRAM, macros, and library cell designs.

To learn more about Synopsys solutions, please visit booth number 616 during TSMC 2019 Open Innovation Platform® Ecosystem Forum at the Santa Clara Convention Center, Santa Clara, California on September 26, 2019.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

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