Synopsys Extends Portfolio of Cloud Computing IP with 112G Ethernet PHY for Hyperscale Data Center SoCs

DesignWare 112G Ethernet PHY on TSMC's N7 Process Enables True Long Reach Channels for 800G Networking Applications

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Highlights:

- 112G Ethernet PHY IP, based on Synopsys' silicon-proven 56G Ethernet IP, offers more than 35dB channel loss for optical, copper cables, and backplane interconnects
- Optimized IP layout maximizes bandwidth per die-edge through stacking and placement on all 4 edges of the die for dense SoC designs
- Unique architecture supports independent, per lane data rates for ultimate flexibility to address broad range of protocols and applications
- ADC- and DSP-based architectures support power scaling techniques, delivering up to 20% power reduction in low-loss channels

Synopsys, Inc. (Nasdaq: SNPS) today announced its DesignWare® 112G Ethernet PHY IP on TSMC's N7 process supporting true long reach channels for up to 800G networking applications. The DesignWare 112G PHY, based on Synopsys' silicon-proven 56G Ethernet PHY available in multiple FinFET processes, delivers PAM-4 signaling for more than 35dB channel loss across optical, copper cables, and backplane interconnects. The 112G PHY's unique transmit phase-locked loop architecture allows independent, per lane data rates for a broad range of high-throughput protocols and applications. To maximize bandwidth and beachfront density, the 112G PHY's flexible layout allows placement of square macros in a multi-row structure and along all edges of the die. Combined with Synopsys' routing feasibility study, packages substrate guidelines, signal and power integrity models, and thorough crosstalk analysis, Synopsys provides a comprehensive 112G Ethernet PHY solution for fast, reliable integration into hyperscale data center SoCs. The DesignWare 112G Ethernet PHY extends Synopsys' portfolio of IP for cloud computing applications, including widely-used protocols such as PCI Express®, DDR, HBM, CCIX, and more.

"Synopsys has been a long-term ecosystem partner in enabling the design community with a comprehensive portfolio of high-quality IPs supporting many generations of TSMC's process technologies," said Suk Lee, senior director of the Design Infrastructure Management Division at TSMC. "We're pleased to see the availability of Synopsys' DesignWare 112G Ethernet PHY IP on TSMC's industry-leading N7 process to address the customer's requirements on aggressive power and performance for a successful silicon innovation."

The 112G Ethernet PHY incorporates Synopsys' silicon-proven data converters, and implements power scaling techniques for up to 20 percent power reduction in low-loss channels. The comprehensive test features, including embedded bit-error rate tester and internal eye monitor, provide on-chip testability and visibility into channel performance. The 112G Ethernet PHY delivers robust performance across voltage and temperature variations using continuous calibration and adaptation algorithms.

"For more than two decades, Synopsys has led the industry with trusted IP solutions that enable our customers to achieve their most challenging power and performance goals for their SoC designs," said John Koeter, vice president of marketing for IP at Synopsys. "The launch of our 112G Ethernet PHY on TSMC's advanced N7 process addresses the demanding high throughput requirements of AI, cloud computing, and networking designs, while significantly lowering integration risk."

Availability and Additional Resources

The DesignWare 112G Ethernet PHY for TSMC's N7 process is scheduled to be available in Q1 of 2020.

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes logic libraries, embedded memories, embedded test, analog IP, wired and wireless interface IP, security IP, embedded processors, and subsystems. To accelerate prototyping, software development, and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP prototyping kits, IP software development kits, and IP subsystems. Synopsys' extensive investment in IP quality, comprehensive technical support, and robust IP development methodology enable designers to reduce integration risk and accelerate time-to-market. For more information on DesignWare IP, visit http://www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

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