Synopsys Delivers Industry's First Compute Express Link (CXL) IP Solution for Breakthrough Performance in Data-Intensive SoCs

DesignWare CXL IP Delivers Low Latency and High Bandwidth for Artificial Intelligence, Memory Expansion, and Cloud Computing Applications

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Highlights:

- Complete DesignWare CXL IP solution is built on Synopsys' silicon-proven PCI Express 5.0 IP, lowering integration risk for device and host applications
- 512-bit CXL controller enables a highly efficient x16 link for maximum bandwidth with extremely low latency
- Silicon-proven 32 GT/s PHY allows for more than 36 dB channel loss across PVT variations for long reach applications
- VC Verification IP for CXL verifies I/O, memory access, and coherency protocol features for all link configurations up to 16 lanes and 32 GT/s data rates
- Synopsys' CXL controller, PHY, and verification IP solution is compliant with the CXL 1.1 specification, supporting all required CXL protocols and device types

Synopsys, Inc. (Nasdaq: SNPS) today announced availability of its complete DesignWare® Compute Express Link (CXL) IP solution consisting of controller, PHY, and verification IP for AI, memory expansion, and high-end cloud computing system-on-chips (SoCs). The CXL protocol enables low-latency data communication between the SoC and general-purpose accelerators, memory expanders, and smart I/O devices requiring high-performance, heterogenous computing for data-intensive workloads. Synopsys' DesignWare CXL IP solution is compliant with the CXL 1.1 specification and supports all three CXL protocols (CXL.io, CXL.cache, CXL.mem) and device types to meet specific application requirements. The CXL IP is built on Synopsys' DesignWare IP for PCI Express 5.0, which has been adopted by more than a dozen leading semiconductor companies across all key market segments and has demonstrated proven interoperability with a range of products in the ecosystem.

"Compute Express Link is a key enabler for next-generation heterogeneous computing architectures, where CPUs and accelerators work together to deliver the most advanced solutions," said Dr. Debendra Das Sharma, Intel Fellow and director of I/O Technology and Standards at Intel. "With support from leading IP providers like Synopsys, we're well on the way to a robust, innovative CXL ecosystem that will benefit the whole industry."

Synopsys' DesignWare CXL Controller helps designers achieve timing closure at 1GHz and provides a robust 512-bit architecture that supports x16 links for maximum CXL bandwidth. In addition, the CXL Controller offers reliability, availability, serviceability (RAS) capabilities to help maintain data reliability, as well as successfully debug and resolve linkup issues. The 32 GT/s PHY allows more than 36 decibel (dB) channel loss across power, voltage, and temperature (PVT) variations for challenging long-reach applications. The VC Verification IP for CXL verifies I/O, memory access, and coherency protocol features with built-in sequences, checks, and coverage for all link configurations up to 16 lanes and 32 GT/s data rates. SystemVerilog test suites for CXL accelerate verification closure and are available as source code.

"As the leader in interface IP, Synopsys continues to stay in the forefront of developing IP for new generations of interconnects such as CXL to help designers incorporate the necessary functionality into their SoCs," said John Koeter, vice president of marketing for IP at Synopsys. "We have leveraged our expertise in PCI Express 5.0 to bring our complete DesignWare CXL IP solution to market and enable designers to meet the memory coherency and fast data connectivity requirements of their SoC with less risk."

Availability and Resources

Synopsys' 32G PHY IP for CXL is available now in 16-nm, 10-nm, and 7-nm FinFET processes. The CXL Controller and VC Verification IP for CXL are available now.

For more information, visit the DesignWare CXL IP and Verification IP web pages.

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes logic libraries, embedded memories, embedded test, analog IP, wired and wireless interface IP, security IP, embedded processors and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP prototyping kits, IP software development kits and IP subsystems. Synopsys'

extensive investment in IP quality, comprehensive technical support and robust IP development methodology enable designers to reduce integration risk and accelerate time-to-market. For more information on DesignWare IP, visit http://www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

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