Synopsys Extends Leadership with Enhanced Verification Continuum Platform

New Native Tool Integrations Enable up to 5X Higher Verification Performance

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Highlights:

- Smart Loading technology in Verdi, enabled by Unified Compile with VCS, delivers 5X faster design load and tracing
- Unified constraint solver technology in VC Verification IP enables 2X higher simulation performance with VCS
- Native integration of VC Formal testbench analyzer application and Certitude enables 10X faster quality assessment of testbench and assertions
- New VC Accelerated Verification IP combined with native integration of VCS and ZeBu increases simulation performance by 10-100X

Synopsys, Inc. (Nasdaq: SNPS) today announced a new release of its Verification Continuum™ Platform with new native integrations across verification tools, enabling up to 5X higher verification performance. Verification Continuum is built from the industry's fastest engines developed by Synopsys, including Virtualizer™ virtual prototyping, SpyGlass® static and VC Formal® verification technologies, VCS® simulation, ZeBu® emulation, Synopsys HAPS® prototyping, Verdi® debug, and VC Verification IP (VIP). Increasing system-on-chip (SoC) complexity, growing SoC software content, and rising time-to-market pressures are driving the need for a highly-efficient verification platform. New enhanced native integrations in Verification Continuum enable performance gains between all verification engines, accelerating time-to-market for complex SoC designs.

"Innovium's highly innovative and production-ready TERALYNX™ data center Ethernet switch silicon delivers speeds of 2 Terabits-per-second to 12.8 Terabits-per-second," said Avinash Mani, vice president of engineering at Innovium. "To meet our aggressive targets, we took advantage of the industry-leading performance of Synopsys' VCS working together with its VC Verification IP for Ethernet and source code test suites to accelerate the tapeout schedule of our market-leading switch products."

"To gain a competitive edge, we needed a comprehensive solution to improve our verification flow and reduce time-to-market for our high-performance AI solutions," said Bin Liang, vice president at Iluvatar. "Synopsys' VC Formal control and datapath applications, combined with native compile in VCS and unified debug in Verdi, enabled us to uncover dead code in minutes and prove a complex 128 x 128 MAC in one day."

New Native Integrations

- Simulation and Debug—The new Verdi release delivers Smart Loading technology, enabled by Unified Compile with VCS, that speeds Verdi design load time by 5X. Additionally, enhanced native multi-threaded dumping cuts overhead by 50 percent, and the new dynamic waveform aliasing technology enables 3X smaller FSDB size.
- Static Verification, Simulation, and Debug—Native integration of SpyGlass and VCS Unified Compile enables seamless read of DesignWare® IP and encrypted IP designs, significantly improving ease-of-use compared to previous black-box support of IP. In addition, integration of Verdi's Unified Debug interface with SpyGlass enables a consistent debug user experience across the verification flow.
- Formal Verification and Functional Qualification—The new VC Formal release delivers 2X performance improvement with enhanced engine optimization and orchestration. Native integration of the VC Formal testbench analyzer (FTA) application and Certitude® functional qualification system enables 10X faster quality assessment of testbench and assertions. This is achieved with a single compile and intelligent fault injection and scheduling for formal property verification.
- Simulation and Verification IP—Native integration across VCS and VC Verification IP delivers a 2X speed-up in simulation performance. This is achieved by optimizations between VCS and VC VIP leveraging native UVM technology and industry-leading constraint solver technology.
- Accelerated VIP, Emulation, and Simulation—Unified compile of design and testbench and low latency interface supporting a seamless mix of signal-level and transaction-level communication, combined with native integration of VCS, ZeBu, and Accelerated VIP, deliver 10-100X speed-up in simulation acceleration compared to simulation alone.

"Synopsys' Verification Continuum Platform, built on industry-leading hardware and software verification tools, delivers new native integrations to enable designers to accelerate verification closure," said Ajay Singh, senior

vice president, engineering of the Verification Group at Synopsys. "The significant verification R&D investments Synopsys has made since introducing the platform demonstrate our commitment to helping customers reduce time-to-market by months for advanced SoC designs."

Availability

Availability is scheduled for June 2019.

Additional Resources

For more information on Verification Continuum Platform please visit:
https://www.synopsys.com/verification.html

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

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