IC Compiler II with Advanced Fusion Technologies Delivers Optimal QoR and Reduces ECO Turnaround Time More Than 40% at Juniper Networks

Juniper Networks Achieves 14% Lower Power and 6% Smaller Area on Next-generation Networking Design

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Highlights:

- Exceptional QoR delivered by IC Compiler II with Advanced Fusion technologies enables Juniper to meet aggressive PPA goals for next-generation networking designs
- Advanced Fusion technologies for design, signoff, and ECO optimization deliver more than 40% faster ECO time to results (TTR) with hyper-convergent design closure

Synopsys, Inc. (Nasdaq: SNPS) today announced that its innovative IC Compiler™ II place-and-route solution with Advanced Fusion technologies has been deployed at Juniper Networks, where it delivered better power and area results. In addition, Engineering Change Order (ECO) turnaround time can be reduced by more than 40 percent when performed inside the IC Compiler II place-and-route solution. IC Compiler II and Advanced Fusion technologies, key components of the Synopsys Fusion Design Platform™, enable unique optimization capabilities for better quality of results (QoR) with golden signoff accuracy during implementation. Designs utilizing Advanced Fusion technologies result in significantly improved correlation to power, timing, and rail signoff engines, while minimizing the number of ECO iterations required for design closure.

Juniper Networks is expanding usage of IC Compiler II with Advanced Fusion technologies as a solution to provide additional power and reliability required for its next-generation 7-nanometer (nm) system-on-chip (SoC) networking design that is comprised of billions of transistors. To achieve six percent (6%) area and fourteen percent (14%) power savings, Juniper Networks deployed several IC Compiler II technologies, such as multibit banking, low power placement, concurrent clock and data (CCD) optimization, and mesh-based clock tree synthesis. Specific Advanced Fusion technologies deployed by Juniper Networks include logic restructuring, which reduced the design area up to three percent (3%) with no impact to timing and power grid augmentation (PGA) for reliability. Used on a portion of their 7nm design tapeout, PGA resulted in 22.5 percent dynamic voltage drop improvement. Juniper also evaluated use of ECO Fusion on a challenging block, which resulted in 43 percent faster TTR along with two percent additional power savings.

"Our silicon is at the heart of all of Juniper's high-performance networking products, which tend to consume greater than 100 watts of power, so our primary objective is to significantly reduce power on our designs," said Narayan Subramaniam, ASIC methodology lead at Juniper Networks. "Deployment of all of the latest IC Compiler II and Advanced Fusion technologies has helped us to achieve optimal PPA by reducing the area and power with no impact on timing on our 7-nanometer tapeout. In addition, out-of-the-box clean signoff timing is another one of our major goals, so, we expect that ECO Fusion will help to further reduce TTR while providing additional QoR improvements."

Announced approximately a year ago, Advanced Fusion technologies have recently been enhanced to include more optimization capabilities, such as logic restructuring for optimal power, performance, and area (PPA), IR-drop-driven placement and optimization, PrimeTime® delay calculation with exhaustive Path Based Analysis (PBA), and signoff-accurate ECO. Used within the IC Compiler II environment, Advanced Fusion technologies deliver unsurpassed QoR and design convergence.

"IC Compiler II with Advanced Fusion Technologies has delivered the best PPA while proving that ECO iterations and turnaround time can be reduced by 40 percent," said Sanjay Bali, senior director of marketing in the Design Group at Synopsys. "Juniper Networks is a leader in providing advanced networking solutions, and their deployment of IC Compiler II with Advanced Fusion technologies is key to helping them deliver lower-power silicon that is better for the environment at a lower cost."

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

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