Synopsys and Arm Extend Collaboration to Fusion Compiler to Accelerate Implementation of Arm's Next-Generation Client and Infrastructure Cores

QuickStart Implementation Kits Enhanced to Enable Fusion Compiler to Speed Implementation and Improve PPA for Arm-based SoCs

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Highlights:

- Collaboration benefits demonstrated with successful SoC tapeouts by early adopters of Arm's latest Cortex-A76 and Neoverse N1 processors using Synopsys' Fusion Design Platform
- Synopsys' QuickStart Implementation Kits (QIKs) being enhanced to use Fusion Compiler to deliver optimum PPA for key cores, including next-generation Arm processors
- Video of the Arm/Synopsys session at Silicon Valley Synopsys Users Group (SNUG) outlining best practices for implementing the latest Arm processors available at https://solvnet.synopsys.com/retrieve/3063262.html

Synopsys, Inc. (Nasdaq: SNPS) today announced that Synopsys and Arm have expanded their collaboration to deliver QuickStart Implementation Kits (QIKs) supporting Synopsys' Fusion Compiler™ solution, the industry's only fully-integrated RTL-to-GDSII implementation system. Architected to deliver the fastest time-to-results (TTR) and to improve power, performance, and area (PPA) for Arm®-based processors, Fusion Compiler accelerates implementation for earliest realization of customers' highly-differentiated products containing Arm's new and future core architectures. This latest work builds on earlier collaborations that led to successful early-adopter tapeouts of system-on-chips (SoCs) incorporating Arm's Cortex®-A76 and Neoverse™ N1 processors.

"Arm and Synopsys have enjoyed more than 25 years of successful collaboration, enabling designers to get innovative products to market quickly while meeting power, performance, and area targets," said Ian Smythe, vice president of marketing, Client Line of Business, Arm. "This latest phase of our collaboration will ensure that designers deploying Synopsys' Fusion Compiler can accelerate development of their differentiated products based on Arm's next generation of processors across the entire compute spectrum, from mobile devices to cloud infrastructure."

Arm and Synopsys collaborate to build QIKs, which include scripts and reference guides, to capture the best practices for implementing key Arm processors using Synopsys' Fusion Design Platform™, now including Fusion Compiler. Synopsys' QIKs also take advantage of Arm Artisan® Physical IP and POP™ IP. Arm and Synopsys recently co-presented some of these best practices as applied to the Cortex-A76, Neoverse N1, as well as future processors at the Synopsys Users Group (SNUG®) in Silicon Valley. Designers can view a recording of this presentation at https://solvnet.synopsys.com/retrieve/3063262.html.

"Fusion Compiler, an integral part of the Fusion Design Platform, offers a highly-differentiated solution to realize the optimum PPA demanded by applications targeted by Arm's next-generation cores," said Deirdre Hanford, co-general manager of the Design Group at Synopsys. "By expanding our implementation collaboration with Arm to incorporate Fusion Compiler, we aim to accelerate industry deployment of the best-in-class quality of results and fastest design convergence that is delivered by the industry's only RTL-to-GDSII solution."

Fusion Compiler, the latest product in the Synopsys Fusion Design Platform, has been uniquely architected to enable design teams to achieve the optimal levels of PPA in the most convergent manner to ensure the fastest and most predictable TTR. Deploying a single, highly-scalable data model and natively integrating an analysis backbone that leverages technology from the industry's golden signoff analysis tools, Fusion Compiler guarantees that critical PPA metrics are optimized efficiently and effectively throughout the full RTL-to-GDSII design flow. Fusion Compiler enables best-in-class PPA through a highly-leveraged and converged optimization framework, resulting in a fully-unified physical synthesis and optimization methodology where industry-leading Synopsys technologies can be deployed at any point throughout the flow for maximum effect and optimal overall convergence. This groundbreaking approach enables up to 20 percent better timing quality-of-results (QoR), 10-15 percent better total power, and up to 5 percent better area compared to using a classic combination of front- and back-end tools. Additionally, Fusion Compiler's unrivaled capacity enables SoC-level global design planning, which offers innovative hierarchical design flows for enhanced productivity.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

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