Synopsys Design Platform Certified for TSMC's Innovative SoIC Chip Stacking Technology

Close Collaboration Delivers Design Solutions for True 3D Device Integration

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Highlights:

- Efficient support for the new chip stacking technology ensures realization of highest-performing 3D-IC solutions
- Solution includes multi-die layout implementation, as well as parasitic extraction and timing analysis coupled with physical verification
- Collaborating with early partners to accelerate their highly integrated, next-generation products to market

Synopsys, Inc. (Nasdaq: SNPS) today announced that the Synopsys Design Platform has been certified for TSMC's latest System-on-Integrated-Chips (TSMC-SoIC™) 3D chip stacking technology. The platform-wide enablement, combined with a highly flexible reference flow, enables immediate customer deployments for high-performance, high-connectivity, multi-die technology solutions spanning mobile computing, network communication, consumer, and automotive electronics applications.

Centered around Synopsys' design implementation and signoff solutions, the high-capacity reference methodology includes advanced through-dielectric-via (TDV) modeling, multi-die layout capture, physical floorplanning, and implementation, as well as parasitic extraction and timing analysis and highly-scalable physical verification. Key products and features of the Synopsys Design Platform supporting TSMC's advanced SoIC chip stacking technology include:

- **IC Compiler™ II place-and-route:** Efficient design capture and flexible planning of high-complexity multi-die ICs. High-quality, routing support encompassing TSV, TDV, bump, and RDL connectivity solutions.
- **PrimeTime® timing signoff:** Full-system static timing analysis, supports multi-die static timing analysis (STA).
- **StarRC™ extraction signoff:** Advanced features for 3D-IC methodologies to handle multi-die parasitic interaction and new modeling for TDV and TSV.
- **IC Validator physical signoff:** DRC and LVS verification, including support for SoIC cross-die interface DRC/LVS checking.

"With system bandwidth and complexity challenges demanding new innovation, TSMC has once again delivered the new 3D-integration technology targeted to bring efficient implementation of highly-differentiated products to market," said Suk Lee, TSMC senior director, Design Infrastructure Management Division. "Our ongoing collaboration with Synopsys results in delivering scalable methodologies for TSMC's innovative SoIC advanced chip stacking technology. We look forward to our mutual customers benefiting from these advanced technology and services for truly systems-in-package."

"The fruits of our latest collaboration with TSMC promise to deliver groundbreaking advances in system size and available system performance," said Sassine Ghazi, co-general manager of Synopsys' Design Group. "Synopsys' digital design platform and the co-developed associated methodologies will allow designers to confidently meet their schedules when deploying these next-generation, multi-die solutions."

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

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