TSMC Certifies Synopsys' Digital and Custom Design Platforms on TSMC 5nm FinFET Process Technology

Production-ready Flow Enables High-performance Compute and Mobile Applications

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Highlights:

- IC Compiler II and Design Compiler Graphical provide a complete digital implementation flow delivering optimized power, performance, area, and full via pillar support
- StarRC, PrimeTime, NanoTime, and PrimeTime PX enable full-flow implementation and signoff support for extraction, timing, and power
- Synopsys' Custom Design Platform with advanced simulation solution supports new 5nm design rules and FinFET device models

Synopsys, Inc. (Nasdaq: SNPS) today announced that TSMC has certified both the Synopsys digital and custom design platforms on TSMC's latest production-ready Design Rule Manual (DRM) for its industry-leading 5-nanometer (nm) FinFET process technology. With several test chips taped out and production designs currently under development by multiple customers, this certification enables a wide range of designs spanning high-performance compute to ultra-low-power, mobile applications. This certification is the result of an extensive, multi-year collaboration with rigorous validation to deliver a design solution for optimized power, performance, and area that speeds the path to next-generation designs.

Synopsys Design Compiler® Graphical synthesis and IC Compiler™ II place-and-route tools have been enhanced to enable designers to take full advantage of TSMC's 5nm FinFET process with extended support for advanced via-pillar implementation, multi-bit flip-flop (MBFF) banking/debanking, and leakage-power optimization. PrimeTime® timing analysis has also been advanced to support cross-cell placement constraints and timing-driven physically-aware static timing analysis (STA) engineering change orders (ECO). Through a close collaboration with TSMC, full-flow correlation was ensured from place-and-route to timing and physical signoff for all the 5nm EUV enablement features.

"Our ongoing collaboration with Synopsys and early customer engagements on TSMC's industry-leading 5nm FinFET process technology result in delivery of platform solutions that enable our mutual customers to quickly launch their new product innovations to market," said Suk Lee, senior director of the Design Infrastructure Management Division at TSMC. "Certification of the Synopsys design platforms enables our mutual customers' designs to be implemented on our production-ready, EUV-enabled 5nm process technology."

"Our collaboration with TSMC on their industry-leading 5nm FinFET process allows customers to confidently begin designing their increasingly large SoCs using Synopsys' highly-differentiated digital and custom design platforms," said Sassine Ghazi, co-general manager of Synopsys' Design Group. "The result of our collaboration enables designers to benefit from significant power, performance, and area improvements of an advanced EUV process, while accelerating time-to-market for their differentiated SoCs."

Synopsys technology files are available from TSMC for the 5nm technology process. Key products and features of the Synopsys design platforms certified by TSMC on its 5nm FinFET process with EUV Lithography include:

- **IC Compiler II place-and-route:** Fully automated, full-color routing and extraction support coupled with extended via-pillar automation. Deployment of next-generation placement and legalization technologies including advanced pin-access modeling to support aggressive cell footprint shrinks and enable higher design utilizations.
- **PrimeTime timing signoff:** Advanced variation modeling for low voltages, and enhanced ECO technologies with support for new physical design rules.
- **PrimeTime PX power signoff:** Advanced power modeling to accurately analyze leakage effects of ultra-high-density standard-cell designs.
- **StarRC™ extraction signoff:** Advanced modeling to handle the complexity of 5nm devices, as well as a common technology file for parasitic extraction consistency from synthesis to place-and-route to signoff.
- **IC Validator physical signoff:** Qualified DRC, LVS, and fill runsets developed natively. DRC runset released at the same time that TSMC released the design rules.
- **HSPICE®, CustomSim™, and FineSim® simulation solutions:** FinFET device modeling with Monte Carlo feature support, and accurate circuit simulation results for analog, logic, high-frequency, and SRAM designs.
- **CustomSim reliability analysis:** Accurate dynamic transistor-level IR/EM analysis for 5nm EM rules.

- **Custom Compiler™ custom design:** Support for new 5nm design rules, coloring flow, poly track regions, and new MEOL connectivity requirements.
- **NanoTime custom timing signoff:** Runtime optimization for 5nm devices, POCV analysis for FinFET stacks, and enhanced signal integrity analysis for custom logic, macros, and embedded SRAMs.
- **ESP-CV custom functional verification:** Transistor-level symbolic equivalence checking for SRAM, macros, and library cell designs.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

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