Synopsys Unveils IC Validator NXT to Cut Physical Signoff Cycle by 2X

Breakthrough Explorer DRC, Live DRC, and Fusion Technologies Deliver Unparalleled Productivity Gains

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Highlights:

- Industry-leading scalability to 2000+ cores enables full-chip physical signoff within hours
- Innovative Explorer DRC technology delivers 5X faster DRC performance during SoC integration
- IC Validator NXT physical signoff deployed in the cloud on multiple customer tapeouts
- Faster physical signoff closure driven by Fusion Technology with IC Compiler II and Live DRC with Custom Compiler

Synopsys, Inc. (Nasdaq: SNPS) today announced its next-generation IC Validator NXT physical verification solution that enables design teams to cut their physical signoff cycle by 2X for advanced technology nodes. IC Validator NXT offers unique technology innovations to address increasingly important productivity needs for physical verification engineers. IC Validator NXT's massively parallel distributed processing architecture and scalability to 2000+ CPUs enables full-chip physical signoff within hours. The new breakthrough Explorer DRC technology offers 5X faster runtime with 5X fewer CPUs and order-of-magnitude debugging speed-up with heatmap for design rule checking (DRC) during chip integration. IC Validator NXT has been successfully deployed in the cloud by multiple customers to meet their aggressive tapeout schedules. IC Validator NXT's Live DRC technology with Custom Compiler™ delivers on-the-fly DRC feedback within seconds and enables an interactive design-and-verify flow.

"As designers adopt 7-nanometer and newer technology nodes, physical verification closure within schedule is becoming a major challenge, and tapeout delays can have a significant impact on our customers' product lifetime revenue and profitability," said Dan Page, vice president, Design Group at Synopsys. "Our new IC Validator NXT technology innovations deliver breakthrough performance scalability and visualization, and provide designers with the fastest path to production silicon."

IC Validator, a key component of Synopsys' Fusion Design Platform™, is a comprehensive and highly scalable physical verification tool suite including DRC, LVS, PERC, dummy metal fill, and design-for-manufacturability (DFM) enhancement capabilities. IC Validator is architected for high performance and scalability that maximizes utilization of mainstream hardware, using smart memory-aware load scheduling and balancing technologies. It uses both multi-threading and distributed processing over multiple machines to provide scalability benefits that extend to more than two thousand CPUs.

Synopsys customers can learn more about the benefits derived from using Synopsys' latest IC Validator technology by attending the upcoming Synopsys Users Group (SNUG®) Silicon Valley event on March 20-21, 2019 at the Santa Clara Convention Center.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

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