Synopsys Fusion Design Platform Enables Successful Tapeout of Samsung Foundry's Industry-first Gate-All-Around Transistor SoC

Close Collaboration Drives Continuous Innovation to Accelerate Next-generation Process Technology

MOUNTAIN VIEW, Calif., Feb 20, 2019 /PRNewswire/ --

Highlights:

- Extensive collaboration enables Synopsys and Samsung Foundry to introduce next-generation transistor technology with successful silicon validation of gate-all-around FET
- Full-flow validation of target power, performance, and area achieved with Synopsys' Fusion Design Platform that includes Design Compiler, IC Compiler II, PrimeTime, and StarRC
- IC Compiler II delivers effective process-enablement pathfinding, key to demonstrating the viability of this next-generation technology

Synopsys, Inc. (Nasdaq: SNPS) today announced that Synopsys' Fusion Design Platform™, including the IC Compiler™ II place-and-route system, has enabled the successful tapeout of Samsung Foundry's industry-first gate-all-around (GAA) system-on-chip (SoC) test chip comprising several high-performance, multi-core subsystems. Building on numerous successful process and design enablement partnerships, this important milestone validates the readiness of GAA transistor architecture, the next-generation transistor technology to support the demands of advanced semiconductor designs. Made possible through IC Compiler II's highly-extensible architecture and ability to efficiently absorb the challenges related to shrinking process geometries, this latest breakthrough further demonstrates IC Compiler II's status as the industry's preferred solution for advanced process node enablement.

"Samsung Foundry has achieved many industry firsts in our drive to deliver differentiated process technology offerings to our comprehensive customer base. The latest tapeout, our GAA test chip, provides further validation of our continued commitment," said Jaehong Park, executive vice president of Design Platform Development at Samsung Electronics. "The agile and fruitful collaboration, which has delivered this technical breakthrough, underscores Synopsys' position as one of the key industry innovators and trusted technology partners."

Emerging challenges at the leading edge of process scaling demands an enhanced inter-developmental working model between the EDA industry and the foundry. Optimizing solutions to address complexities introduced by advanced process technology that include increased transistor densities and utilization, design rules and routability, and growing variability, is paramount to achieving new node success. Advanced extreme ultraviolet (EUV) manufacturing technology provides significant help in mitigating some of these complexities, however increasing layout-dependent effects and thus inter-cell dependencies have demanded greater innovation. Samsung Foundry's and Synopsys' work on high-utilization routability and the associated patterning methodology has provided a strong platform that is key to ensuring the viability of this new node. Additionally, multi-year enhancements in IC Compiler II that tightly couple the technologies that span the breadth of the placement, legalization, and routing stages of the design flow have been key to Samsung Foundry achieving its overall logic-area shrink goals for this process. A key benefit of Samsung Foundry's GAA technology is the realization of enhanced gate control and reduced internal transistor parasitics that together demand next-generation optimization technologies to extract the process' combined power,

performance, and area (PPA) potential. Delivered through the continuous infusion of Synopsys' PrimeTime® timing and StarRC™ parasitic-analysis technologies, IC Compiler II's signoff-correlated analysis engines augment its industry-leading, full-flow, total-power-driven optimization framework, ensuring an accelerated and convergent path to targeted PPA. To learn more about the Fusion Design Platform, visit www.synopsys.com/fusion.

"Synopsys prides itself on its long history of enabling the most complex designs and also playing a lead role in enabling advanced processes to deliver the next generation of high-performance SoCs," said Sassine Ghazi, co-general manager, Design Group at Synopsys. "Samsung Foundry has proven to be a visionary collaborator, and the deployment of IC Compiler II and the Synopsys Fusion Design Platform for this gate-all-around technology is a strong affirmation of our continued investments in highly-differentiated innovation as well as our partnership-driven approach to industry leadership."

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

Editorial Contact:
James Watts
Synopsys, Inc.
650-584-1625
jwatts@synopsys.com

SOURCE Synopsys, Inc.