Synopsys and imec Demonstrate Accelerated Modeling of Innovative Complementary FET (CFET) Technology

Partnership Aims to Reduce Parasitic Variation at Sub-3nm Processes

MOUNTAIN VIEW, Calif., Dec 10, 2018 /PRNewswire/ --

Highlights:

- Powerful QuickCap NX 3D field solver interface allows focused experimentation and faster turnaround time
- Novel modeling of delay sensitivity to parasitic variation accurate to within user-specified targets
- Continued collaboration aims to ramp-up advances towards 2nm development

Synopsys, Inc. (Nasdaq: SNPS) announced today another milestone in its longstanding partnership with imec, a world-leading research and innovation hub in nanoelectronics and digital technologies, with the successful completion of the first comprehensive sub-3 nanometer (nm) parasitic variation modeling and delay sensitivity study of complementary FET (CFET) architectures. With the potential to significantly reduce area versus traditional FinFETs, CFET is a promising option to maintain area scaling beyond 3nm technology.

In 3-nm and 2-nm process technologies, the magnitude of variation increases significantly for middle of line (MOL) parameters, as well as interconnect, due to high resistance of metal lines, vias, and surface scattering. Therefore, modeling parasitic variation and sensitivity is a critical factor in bringing CFET to mainstream production.

Prediction at early stages of process development will allow foundries to create more robust and variation-tolerant transistors, standard cells, and methodologies for metal interconnect. Using the QuickCap® NX 3D field solver, in a close collaboration between Synopsys R&D and imec research teams, allowed for fast and accurate modeling of parasitics for a variety of device architectures and to identify the most critical device dimensions and properties. This allowed the optimization of CFET devices for better power/performance trade-offs. As part of a comprehensive set of tools that includes Raphael™ TCAD extraction to StarRC™ parasitic extraction for the largest system-on-chips (SoCs), QuickCap NX effectively helps process engineers understand the sensitivity of circuit performance to variations in process parameters and improves modeling accuracy by establishing golden reference values.

"This work has allowed us to accurately model and analyze cell and interconnect variation at advanced processes and architectures, such as Complementary FET," said Anda Mocuta, director, Technology Solutions and Enablement at imec. "Our collaboration with Synopsys continues a legacy of successful collaborations that enable us to search for technological breakthroughs below 3 nanometers. The capabilities of Synopsys tools, such as QuickCap NX, have been key to our joint research on variability."

"Imec is at the forefront of research into semiconductor technology. Our collaboration with imec to develop variation-aware solutions down to 2 nanometer processes will benefit the entire semiconductor industry," said Antun Domic, chief technology officer at Synopsys. "Utilizing the flexibility of Synopsys' QuickCap NX 3D parasitic extraction interface, engineers can better target and significantly reduce the number of trials needed to optimize circuit performance in the presence of process variation and reduce circuit sensitivity. This significantly reduces the overall turnaround time for device and circuit optimization."

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

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