Synopsys Unveils Fusion Compiler, Enabling 20 Percent Higher Quality-of-Results and 2X Faster Time-to-Results

Innovative RTL-to-GDSII Product Redefines IC Design through Fusion of Synthesis and Place-and-Route

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Highlights:

- Fusion Compiler is the industry's only RTL-to-GDSII product architected with a single, scalable data model, best-in-class optimization engines, and an analysis backbone based on the industry's golden signoff tools
- Fusion Compiler is the only single-cockpit solution for RTL-to-GDSII implementation, unleashing the highest productivity and flexibility for design engineers
- Fusion Compiler's unique architecture shares all technologies across synthesis and place-and-route to enable unprecedented design convergence
- The new tool is deployed at leading semiconductor companies with successful tapeouts at emerging and established nodes

Synopsys, Inc. (Nasdaq: SNPS) today unveiled Fusion Compiler™, an innovative RTL-to-GDSII product that enables a new era in digital design implementation. By fusing a novel high-capacity synthesis technology with the IC Compiler™ II industry-leading place-and-route technology, Fusion Compiler offers new levels of predictable quality-of-results (QoR) to address the challenges presented by the industry's most advanced designs. This unified architecture shares technologies across the RTL-to-GDSII flow to enable a highly convergent system delivering 20 percent better QoR and 2X faster time-to-results (TTR). Fusion Compiler is tapeout-validated at market-leading semiconductor companies and has been proven to deliver the highest-quality designs. Fusion Compiler also enables a single cockpit for RTL-to-GDSII implementation, enabling unparalleled levels of design productivity, flexibility, and throughput to maximize power, performance, and area (PPA) for the most challenging designs.

"Enablement of the next generation of market-shaping products has demanded reassessment of how design productivity and quality-of-results can be improved," said Sassine Ghazi, co-general manager of the Design Group at Synopsys. "Leveraging the leading technologies from IC Compiler II and fusing novel, high-capacity synthesis and our industry-leading golden signoff technologies onto the same scalable data model, Fusion Compiler is engineered to offer the best QoR in the shortest time."

"We have focused on strengthening the product development process from timing design to physical design. As a part of this effort, we evaluated adopting the new Fusion Compiler tool for SoC-based designs. Because of our successful evaluation results, we accelerated the deployment of the tool to a real design," said Seiichi Mori, senior vice president, Toshiba Electronic Devices and Storage Corporation. "The power of this technology is essential for the design of tomorrow's FinFET-based automotive applications. With Fusion Compiler, we achieved the target design goal and completed the tapeout. Compared to conventional technology, we confirmed a 33 percent reduction in timing violations, 10 percent area reduction, and 30 percent less leakage power while cutting the design turnaround time in half. We have completed the integration of Fusion Compiler in Toshiba's design environment and have begun to deploy it to upcoming SoC designs."

"As design complexity increases across all our market segments, our key requirement is to achieve the best product performance coupled with the highest levels of predictability," said Michael Goddard, senior vice president, Samsung SARC and ACL. "With Fusion Compiler, we are on track to achieve optimal PPA with up to 10 percent better timing, 10 percent lower leakage, two-to-five percent dynamic power savings, and typically two-to-three percent area reduction for our most challenging design blocks on our imminent tapeout. In addition, the predictable path from synthesis to signoff reduces design iterations, ensuring that we can meet our aggressive product schedules."

Fusion Compiler is built on a single, highly-scalable data model that supports common signoff analysis, optimization, concurrent clock data optimization, clock topology creation, and routing engines. These best-in-class engines form a single unified optimization framework that is central to Fusion Compiler's predictable flow. Its architecture also enables sharing of advanced technologies across the RTL-to-GDSII design flow. Technologies previously used only in place-and-route can now be applied during synthesis, and vice versa, enabling new levels of timing, power, and area.

"Socionext has long been an early adopter of innovative technologies that deliver tangible results to accelerate our time-to-market," said Taichiro Sasabe, general manager, SoC Design Division at Socionext. "Our early assessment of Fusion Compiler shows significantly better full-flow predictability, faster full-flow turnaround time, and better timing QoR compared to the previous approaches. We are collaborating with Synopsys to deploy this innovative RTL-to-GDSII solution, as it will streamline physical design of our mission-critical projects and allow us to bring new products to market much faster."

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

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