Synopsys Advances Test Fusion Technology with Test Points to Reduce Manufacturing Costs and Boost Quality

Accelerates Achieving Test Goals While Meeting Power, Performance, and Area Targets

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Highlights:

- New test points reduce manufacturing test costs by an average of forty percent and increase defect coverage
- Test Fusion delivers significant reduction in test point silicon area and routing congestion
- Test points easily deployed in one step, automatically leveraging SpyGlass DFT ADV, DFTMAX, and Synopsys synthesis products
- Test point technology widely deployed by multiple semiconductor manufacturers

Synopsys, Inc. (Nasdaq: SNPS) today announced the availability of Test Fusion technology with new test point functionality, providing design teams with powerful design-for-test (DFT) circuit modifications to reduce silicon test costs by an average of forty percent and increase defect detection while meeting design targets for power, performance, and area. Test Fusion ensures the test points avoid introducing routing congestion and minimize area impact, in contrast to traditional test point implementation techniques. RTL designers can easily deploy test points with a single step that automatically combines Synopsys' SpyGlass® DFT ADV testability analysis, DFTMAX™ design-for-test, and Synopsys synthesis products, then run TetraMAX® II automatic test pattern generation (ATPG) to create efficient silicon manufacturing tests. The solution is fully certified to comply with the ISO 26262 automotive functional safety standard and is widely deployed among semiconductor manufacturers.

To meet lower cost and increasing quality requirements, semiconductor manufacturers seek new technologies to improve detecting defective silicon prior to shipment. Several industry segments, such as automotive, are challenged to meet manufacturing test cost goals while achieving quality levels for their integrated circuits (ICs) of less than one defective part per million. Synopsys test points assist meeting these requirements by modifying the design to improve the ability of TetraMAX II to generate silicon test programs. SpyGlass DFT ADV analyzes designs and determines the most optimal and effective locations for test points that both decrease test pattern volume and increase defect coverage. Test Fusion technology ensures DFTMAX and Synopsys synthesis tools work in combination to implement the test points at the selected locations while minimizing routing using physical design data. Furthermore, Test Fusion provides an unprecedented reduction of area and congestion by enabling multiple test points to share a single test register based on physical proximity.

"Semiconductor companies are increasingly concerned about meeting manufacturing test quality and cost goals while achieving IC area, power, and performance goals within predictable design schedules," said Steve Pateras, senior director of marketing for Test Automation in Synopsys' Design Group. "Physically-aware test points are just one of several innovative Test Fusion technologies we are bringing to market to address this growing challenge."

For more information on the comprehensive Synopsys Test solution, visitwww.synopsys.com/test.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

Editorial Contact:
James Watts
Synopsys, Inc.
650-584-1625
jwatts@synopsys.com

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