Synopsys Announces Fastest, Most Power Efficient DDR5 and LPDDR5 IP Solutions

New DesignWare Memory Interface IP Targets AI, Automotive, and Mobile SoCs

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Highlights:

- Industry's first LPDDR5 controller, PHY, verification IP solution supports data rates up to 6400 Mbps with up to 40% less area than previous generations
- Complete DDR5 IP solution supports up to 4800 Mbps with single, dual channels for discrete devices and DIMMs
- Both solutions provide several low-power states with short exit latencies, and offer multiple pre-trained states for dynamic frequency change capability

Synopsys, Inc. (Nasdaq: SNPS) today announced new DesignWare® Memory Interface IP solutions supporting the next-generation DDR5 and LPDDR5 SDRAMs. The DDR5 and LPDDR5 IP significantly increase memory interface bandwidth compared to DDR4 and LPDDR4 SDRAM interfaces, while reducing area and improving power efficiency. The DesignWare DDR5 IP, operating at up to 4800 Mbps data rates, can interface with multiple DIMMs per channel up to 80 bits wide, delivering the fastest DDR memory interface solution for artificial intelligence (AI) and data center system-on-chips (SoCs). The industry's first LPDDR5 IP, running at up to 6400 Mbps, provides significant area and power savings for mobile and automotive SoCs with its dual-channel memory interface option that shares common circuitry between independent channels. For additional power savings, the DesignWare Memory Interface IP solutions provide several low-power states with short exit latencies, and offer multiple pre-trained states for dynamic frequency change capability. The DDR5 and LPDDR5 controller and PHY seamlessly interoperate via the latest DFI 5.0 interface, providing a complete memory interface IP solution for high-bandwidth, low-power SoC designs.

"Synopsys and Arm have been collaborating for more than 25 years, helping designers overcome their growing design challenges to drive new innovation," said Dermot O'Driscoll, vice president of Product Solutions, Infrastructure Line of Business, Arm. "Together, we're working to maximize the performance of Arm® Neoverse® designs for infrastructure and cloud by optimizing Synopsys' DDR5 and LPDDR5 IP together with "Zeus" and future CPUs."

The DesignWare DDR5 and LPDDR5 IP solutions support all required features of the DDR and LPDDR specifications, enabling designers to incorporate the necessary functionality into their SoCs:

- Firmware-based training via an embedded calibration processor in the PHY optimizes the boot-time memory training for highest data reliability and margin at the system level. It also allows fast updates to the training algorithms without requiring changes to the hardware
- Decision feedback equalization (DFE) used in the input receivers reduces the impact of intersymbol interference (ISI) to improve signal integrity
- Reliability, availability, serviceability (RAS) features, including inline or sideband error correcting code (ECC), parity, and data cyclic redundancy checks (CRC), reduce system downtime
- Synopsys PHY hardening and signal/power integrity expertise enable faster design completion time and a higher degree of design confidence
- Synopsys VIP for DDR5 and LPDDR5 provides randomized configuration and runtime selection, as

well as built-in comprehensive coverage, verification plan, and protocol checks for increased productivity

"Micron and Synopsys have been working together for many years to address the evolving shift in memory performance requirements for computing applications," said Ryan Baxter, director of Cloud and Verticals at Micron. "The combination of Micron's DRAM devices and Synopsys' memory interface IP blocks solutions enables mutual customers to get a jump-start on their next-generation SoCs for emerging applications in AI, data center, mobile, and automotive that require faster DRAM and new memory interfaces."

"The LPDDR standard is gaining wider adoption in a range of applications beyond high-end mobile, requiring new memory chips to increase DRAM throughput and lower operating voltage," said Sunny Khang, vice president, head of DRAM Product Planning at SK hynix. "Our ongoing collaboration with Synopsys for testing, compatibility, and interoperability of Synopsys' DesignWare LPDDR5 IP with SK hynix' LPDDR5 device will enable our mutual customers to achieve their aggressive power, performance, and area targets."

"Emerging applications such as AI, automotive, and cloud are requiring significantly higher memory bandwidth to address the massive amount of data throughput," said John Koeter, vice president of Marketing for IP at Synopsys. "As the industry's leading provider of DDR IP, Synopsys is offering designers the fastest DDR5 and LPDDR5 IP solutions on the most advanced FinFET processes to deliver innovative products that are differentiated in bandwidth, power, and area."

Availability

- The DesignWare DDR5 PHY and LPDDR5 PHY are scheduled to be available in Q1 of 2019
- The DesignWare DDR5 Controller and LPDDR5 Controller are scheduled to be available in Q2 of 2019
- The VC Verification IP for DDR5 and LPDDR5 is available now.

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes logic libraries, embedded memories, embedded test, analog IP, wired and wireless interface IP, security IP, embedded processors and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP prototyping kits, IP software development kits and IP subsystems. Synopsys' extensive investment in IP quality, comprehensive technical support, and robust IP development methodology enable designers to reduce integration risk and accelerate time-to-market. For more information on DesignWare IP, visit http://www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

Forward-Looking Statements

This press release contains forward-looking statements within the meaning of Section 21E of the Securities Exchange Act of 1934, including statements regarding the expected release and benefits of DesignWare DDR5 PHY and Controller, as well as the LPDDR5 PHY and Controller. Any statements that are not statements of historical fact may be deemed to be forward-looking statements. These statements involve known and unknown risks, uncertainties and other factors that could cause actual results, time frames or achievements to differ materially from those expressed or implied in the forward-looking statements. Such risks and uncertainties include, among others, product timeline and development schedules, or interoperability, performance, and power issues. Other risks and uncertainties that may apply are set forth in the "Risk Factors" section of Synopsys' most recently filed Quarterly Report on Form 10-Q. Synopsys undertakes no obligation to update publicly any forward-looking statements, or to update the reasons actual results could differ materially from those anticipated in these forward-looking statements, even if new information becomes available in the future.

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