Synopsys Custom Compiler Doubles New Customer Adoptions, Introduces New Release

New Fusion Technologies Reduce Time to Analog Design Closure

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Highlights:

- New Extraction Fusion and DRC Fusion technologies enable tighter design/layout collaboration and fewer late-stage design iterations
- Visually-assisted automation proven to deliver 2-10X better productivity
- User community grows to over 3000 designers with significant increase in new customer adoptions

Synopsys, Inc. (Nasdaq: SNPS) today announced that new customer adoptions of its Custom Compiler™ custom design tool doubled in the past year, driven by the proven benefits of its innovative visually-assisted layout automation technologies. Users of Custom Compiler achieved 2-10X improvements in custom design productivity over prior solutions—especially for advanced process nodes. Synopsys also announced the release of the latest version of Custom Compiler, version 2018.09. Custom Compiler version 2018.09 includes performance improvements and enhancements that reduce the time to design closure for custom integrated circuit (IC) design. Significant new features of this release include Extraction Fusion (with StarRC™ technology) and DRC Fusion (with IC Validator technology). These provide custom IC designers with early signoff-quality parasitic feedback during the design process, and signoff-quality design rule checking (DRC) during layout.

New Extraction and DRC Fusion Technologies

Extraction Fusion and DRC Fusion technologies reduce the time it takes to achieve analog design closure. Extraction Fusion enables layout parasitics to be extracted from a partially completed layout. This provides circuit designers and layout designers with earlier feedback of layout parasitics. Circuit designers can use early parasitics to refine their designs and avoid layout rework. Layout designers can use early parasitics to confirm they are meeting design specifications. DRC Fusion enables live design rule checking during layout using IC Validator. By checking for errors during layout, designers can reduce the number of late-cycle iterations caused by design rule violations discovered during final signoff checking.

Visually-assisted Automation Proven to Reduce Layout Time

Custom Compiler's visually-assisted automation technology automates custom layout tasks by leveraging the graphical use model familiar to layout designers, rather than requiring complicated constraint entry and scripting as in competing solutions. Custom Compiler users have been sharing their results from deploying visually-assisted automation in presentations at Synopsys User Group (SNUG®) meetings around the world, and the results have been impressive. In some cases, design time has been reduced by as much as 90%. The latest enhancements further improve user experience and reduce design time, according to feedback from early users.

"Custom Compiler's enhanced Template Assistant enhances our ability to reuse or adapt layouts that are already silicon-proven, giving us better-quality layouts, faster," said Atul Bhargava, senior CAD manager at STMicroelectronics. "Together with the gains achieved by other features of Custom Compiler, we see a significant reduction in the analog layout development cycle. The gain is maximized for analog layouts but is useful for all layouts, in general."

Growing Custom Compiler Customer Adoption

Custom Compiler adoption has been growing rapidly and has now exceeded 3000 users worldwide. Adoption has been driven by customers who value a modern, open platform designed for productivity, especially at advanced nodes.

"proteanTecs invented a novel technology that companions chip products throughout their entire life-cycle, from design, through production, and during service. We chose Custom Compiler to help meet our objective of achieving better PPA, shorter TTM, and dramatically increasing product quality and reliability, while reducing cost," said Yair Talker, proteanTecs vice president of R&D. "We deployed a full-circuit design environment based on Custom Compiler for our 7-nanometer IP and achieved tapeout in just three months. We found Custom Compiler to be a highly productive solution with which to implement our embedded sensors, enabling a plenitude of benefits for our post-silicon SaaS platform that serves the data center and automotive markets."

"Our development focus for this latest release was to improve performance and customer productivity throughout the flow,

especially for design/layout collaboration," said Aveek Sarkar, vice president of the Custom Compiler group at Synopsys. "We worked closely with leading customers and our own internal IP development team to identify and resolve key pain points in the custom IC design flow."

About Synopsys Custom Design Platform

The Synopsys Custom Design Platform is a unified suite of design and verification tools that accelerates the development of robust custom and AMS designs. Anchored by the Custom Compiler custom design environment, the platform features industry-leading circuit simulation performance, a fast, easy-to-use custom layout editor complemented with best-in-class technologies for parasitic extraction, reliability analysis and physical verification.

Key features of the Custom Design Platform include reliability-aware verification, visually-assisted layout, and new Extraction Fusion and DRC Fusion technologies. Reliability-aware verification ensures robust AMS design with signoff-accurate transistor-level EM/IR analysis, large-scale Monte Carlo simulation, aging analysis, and other verification checks. Visually-assisted automation is a pioneering approach to reducing layout effort, especially for advanced-node designs, that is proven to deliver 2-10X higher productivity. Extraction Fusion and DRC Fusion technologies shorten time to design closure and reduce late iterations.

The Synopsys Custom Design Platform is based on the OpenAccess database, includes open APIs for third-party tool integration, and supports programming in TCL and Python. Platform tools include HSPICE® and FineSim® SPICE circuit simulators, CustomSim™ FastSPICE, Custom Compiler layout and schematic editor, StarRC parasitic extraction, and IC Validator physical verification. For more information, visit www.customcompiler.info.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

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