Synopsys Enables Tapeout Success for Early Adopters of Arm Neoverse IP

Synopsys' Design, Verification, Software Integrity, and IP Solutions Enable Power, Performance, Area, and Security Required for Server and Networking Products Based on Arm Neoverse IP

MOUNTAIN VIEW, Calif., Oct. 16, 2018 /PRNewswire/ --

Highlights:

- Early adopters of Arm Neoverse IP, including next-generation "Ares" processor, have successfully taped out using Synopsys' Design Platform with Fusion Technology
- QuickStart Implementation Kits (QIKs), including scripts and reference guide, available today for Arm Neoverse processors in 7-nm process technology
- Synopsys' Verification Continuum Platform accelerates software development, verification closure, and time-to-market for designs based on Arm Neoverse IP
- DesignWare interface IP enables rapid development of secure cloud and network computing Arm-based SoCs

Synopsys, Inc. (Nasdaq: SNPS) today announced that early collaboration with Arm on its next-generation Arm® Neoverse® family of products targeting cloud-to-edge infrastructure has resulted in successful early adopter tapeout in advanced FinFET process technologies using Synopsys' Design Platform with Fusion Technology™, Verification Continuum™ Platform, and DesignWare® interface IP. The collaboration has also produced QuickStart Implementation Kits (QIKs) for Arm's next-generation "Ares" high-performance processor, as well as current Arm Cortex®-A72 and Cortex-A75 processors targeting edge-to-cloud infrastructure systems to enable rapid implementation with optimal quality of results (QoR).

"Arm Neoverse platforms provide a scalable and secure solution foundation for cloud-to-edge infrastructure demanding the highest levels of performance, efficiency, and security," said Drew Henry, senior vice president and general manager, Infrastructure Line of Business, Arm. "We continue to work with Synopsys to enable designers with the latest capabilities of the Synopsys tools and interface IP to achieve their performance, power, area, and security targets for Arm Neoverse SoC designs."

The QIKs, which include implementation scripts and reference guides, take advantage of the latest features in the Synopsys Design Platform with Fusion Technology, enabling designers to achieve their aggressive infrastructure performance, power, and area (PPA) targets faster. The QIKs for Arm Neoverse processors were collaboratively built using Arm Artisan® POP™ technology in 7-nanometer (nm) process technology. Synopsys' Design Platform with Fusion Technology delivers:

- 7nm and below implementation in Design Compiler® Graphical and IC Compiler™ II place-and-route system
- Higher performance with automatic density control and timing-driven placement
- Lower power with full-flow concurrent clock and datapath (CCD) optimization
- Signoff closure with PrimeTime® PBA-based ECO with power recovery and exhaustive PBA along with StarRC™ simultaneous multi-corner extraction
- Early, accelerated design optimization for power integrity and reliability with the RedHawk™ Analysis Fusion signoff-driven flow within IC Compiler II

In addition to QIKs, Synopsys offers design services based on extensive experience in hardening Arm processors to enable companies to reach their aggressive infrastructure and networking processor performance goals. These services range from QuickStart implementation through turnkey core hardening.

Synopsys' Verification Continuum Platform accelerates software development, verification closure, pre-silicon Arm ServerReady compliance testing, and time-to-market for designs based on Arm Neoverse IP. It also enables verification and integration of complex multi-core subsystems, RAM/memory corruption detection, and automated regression for continuous integration to significantly reduce overall testing time. Synopsys verification solutions for Arm Neoverse products include:

- Synopsys ZeBu® emulation with the performance required for SoC-level software bring-up
- Pre-silicon prototyping solutions, including the Synopsys Virtualizer™ Development Kit (VDK) Family for Arm processors, with Arm Fast Models for Cortex-A72, Cortex-A75 and Ares processors, and HAPS® FPGA-based prototypes
- VCS® simulation with fine-grained parallelism technology for Arm Cortex-A processors, and verification IP for Arm

AMBA® interconnect
- Verdi® automated debug system for complex, multi-core server designs

To deliver the required throughput for Arm Neoverse IP, Synopsys provides high-performance, silicon-proven DesignWare interface IP, including PHYs and controllers for DDR, HBM, PCI Express®, CCIX, Ethernet, and USB. Synopsys and Arm have collaborated to optimize the performance of Synopsys DDR and PCI Express IP in Arm-based designs.

Security is central to server and networking products. Arm provides a hardware basis for this security with its Arm Neoverse platforms, and Synopsys' Software Integrity Platform, including Coverity® static application security testing, Defensics® fuzz testing, Seeker® interactive application security testing, and Black Duck software composition analysis, helps secure the software for these complex systems. In addition, Synopsys offers professional services, including a wide range of software security and quality services, to help organizations build security in to their designs.

"Leading semiconductor and system companies rely on Synopsys tools and interface IP for their most advanced cloud, infrastructure, and networking designs," said Deirdre Hanford, co-general manager, Synopsys Design Group. "Synopsys and Arm have been collaborating for more than 25 years to enable mutual customer success, and our latest collaboration delivers optimized support for Neoverse platforms, where our Design Platform with Fusion Technology, Verification Continuum Platform, and DesignWare interface IP have already enabled tapeout success for early adopters of Arm's next-generation "Ares" processor."

Availability
QIKs for key Arm Cortex-A class processors, including Cortex-A72, Cortex-A75, and "Ares" processors, are available today at https://www.synopsys.com/Arm-Opto. The QIK for the "Ares" processor is available today on request from Synopsys. More information about Arm-Synopsys collaboration is available at https://www.synopsys.com/Arm.

About Synopsys
Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

ANSYS, ANSYS Workbench, AUTODYN, CFX, FLUENT and any and all ANSYS, Inc. brand, product, service and feature names, logos and slogans are registered trademarks or trademarks of ANSYS, Inc. or its subsidiaries in the United States or other countries. All other brand, product, service and feature names or trademarks are the property of their respective owners.

Editorial Contact:
James Watts
Synopsys, Inc.
650-584-1625
jwatts@synopsys.com

SOURCE Synopsys, Inc.