Synopsys to Showcase Optimized Solutions and Expert Services for Arm-based Designs at Arm TechCon 2018

MOUNTAIN VIEW, Calif., Oct. 9, 2018 /PRNewswire/ -- Synopsys, Inc. (Nasdaq: SNPS) will showcase its industry-leading Synopsys Design Platform, Verification Continuum™ Platform, and DesignWare® IP at Arm® TechCon at the San Jose Convention Center in San Jose, California, October 16th to 18th. Synopsys offers optimized solutions and expert professional services to accelerate innovation throughout the Arm-based product design flow. Register for a free expo pass or all-access conference pass to Arm TechCon 2018 at https://www.armtechcon.com/registration.html. Use promo code '18ARMSYN' to get $300 off an all-access pass.

Visit Synopsys at Arm TechCon 2018 in Hall 1 & 2, Booth 619

Synopsys will provide a number of demonstrations at its booth and present technical sessions over the course of the conference. Synopsys' sessions on Wednesday, October 17 in room 210-D are free of charge and do not require a conference badge. Synopsys' demonstrations in its expo booth at Arm TechCon 2018 will include DesignWare IP for CCIX and PCI Express, Optimized PPA and Faster TTR for Arm-based SoCs with Fusion Technology™, and Verification Continuum demos.

Synopsys-Arm Collaboration Technical Sessions—Wednesday, October 17, Room 210-D

- Session: HiSilicon Technologies Shares Best Practices to Accelerate Tapeout of Their 7-nm, Arm Cortex-A76 Based High-Performance Mobile AI Computing Chipset
  Speaker: Yangle Wu, HiSilicon Technologies; Ron Duncan, Synopsys
  Time: 11:30 a.m. – 12:30 p.m. PDT
- Session: A Signoff-driven Physical Design Flow for Arm Processors with RedHawk Analysis Fusion in IC Compiler II
  Speaker: Kenneth Chang, Synopsys; Annapoorna Krishnaswamy, ANSYS
  Time: 12:30 p.m. – 1:30 p.m. PDT (Lunch provided)
- Session: Best Practices and Synopsys QuickStart Implementation Kits (QIKs) for the Latest Armv8-A Processors
  Speaker: Mike Montana, Synopsys
  Time: 1:30 p.m. – 2:30 p.m. PDT
- Session: Designing Arm-based SoCs with Next-Generation High-Speed Interfaces
  Speaker: Scott Knowlton, Synopsys
  Time: 2:30 p.m. – 3:30 p.m. PDT
- Session: Can ISO 26262 Random Fault Analysis be Scaled to Complex SoCs Containing Third-Party IP?
  Speaker: Kevin Rich, NVIDIA
  Time: 3:30 p.m. – 4:30 p.m. PDT
- Session: Automated and Scalable Functional Safety Verification is Essential for ISO 26262 Compliance of Automotive SoCs
  Speaker: David Hsu, Synopsys
  Time: 4:30 p.m. – 5:30 p.m. PDT

Conference Sessions—Thursday, October 18, Executive Ballroom 210-H

- Session: Arm-Synopsys Collaboration to Enable Edge-to-Cloud Computing
  Speaker: Rahul Deokar, Synopsys; David Koenen, Arm
  Time: 1:30 p.m. – 2:30 p.m. PDT
- Session: Using Virtual Prototyping for Accurate Performance Analysis – An SSD Controller Case Study
  Speaker: Malte Doerper, Synopsys; Tim Kogel, Synopsys; Jason Andrews, Arm; Eric Sondhi, Arm
  Time: 2:30 p.m. – 3:30 p.m. PDT

Visit the Arm TechCon event page on the Synopsys website for more details.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

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