Synopsys and TSMC Collaborate to Develop Portfolio of DesignWare IP for TSMC N7+ FinFET Process

Successful Customer Tapeouts of DesignWare IP in N7+ Marks Significant Milestone of the Collaboration

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Highlights:

- Tapeouts of DesignWare Logic Libraries, Embedded Memories, USB, DisplayPort, PCI Express, and MIPI M-PHY in N7+ demonstrate high quality and robustness of the IP
- DesignWare PHY IP in development for TSMC N7+ process includes DDR, LPDDR, MIPI D-PHY, Ethernet, and SD/eMMC
- Synopsys STAR Memory System delivers high test coverage of N7+ memories, and STAR Hierarchical System automates porting of manufacturing patterns
- DesignWare IP for TSMC N7+ process enables next wave of high-density, power-efficient mobile and data center SoCs

Synopsys, Inc. (Nasdaq: SNPS) today announced a collaboration with TSMC to develop a broad portfolio of DesignWare® Interface IP, Logic Libraries and Embedded Memories for the TSMC N7+ FinFET process. Multiple customer tapeouts in the N7+ process using Synopsys DesignWare IP demonstrates the high quality and robustness of the IP for TSMC's advanced FinFET process. The combination of TSMC's N7+ process and Synopsys' DesignWare IP helps designers develop the next wave of compact, high-density, low-power mobile and data center system-on-chips (SoCs) with significantly less risk while accelerating their time-to-market.

"TSMC and Synopsys have been collaborating for more than a decade to provide designers with the IP necessary to differentiate their SoCs manufactured in TSMC's FinFET processes," said Suk Lee, senior director of the TSMC Design Infrastructure Marketing Division. "The multiple customer tapeouts of DesignWare IP for TSMC's N7+ process demonstrates Synopsys' continuous commitment in developing high-quality IP that enables designers to meet their design goals while quickly ramping into volume production."

"As the leading provider of physical IP, Synopsys is focused on helping designers implement the latest functionality into their SoCs with IP in the process technology they need, precisely when they need it," said John Koeter, vice president of marketing for IP at Synopsys. "By delivering DesignWare IP for TSMC's N7+ process, Synopsys enables designers to integrate the necessary features into the next era of high-performance, low power mobile and data center SoCs with significantly less risk."

Availability

- DesignWare Logic Libraries, Embedded Memories, and PHYs supporting USB 2.0/3.1, DisplayPort, PCI Express 3.1, and MIPI M-PHY are available now in TSMC N7+
- DesignWare IP for DDR, LPDDR, MIPI D-PHY, PCI Express 4.0/5.0, 25G Ethernet, and SD/eMMC are scheduled to be available in TSMC N7+ in first half of 2019
- The STAR Memory System® and STAR Hierarchical System solutions are available now

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes logic libraries, embedded memories, embedded test, analog IP, wired and wireless interface IP, security IP, embedded processors and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP prototyping kits, IP software development kits and IP subsystems. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enable designers to reduce integration risk and accelerate time-to-market. For more information on DesignWare IP, visit https://www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-

quality, secure products. Learn more at www.synopsys.com.

Forward-Looking Statements

This press release contains forward-looking statements within the meaning of Section 21E of the Securities Exchange Act of 1934, including statements regarding the expected release and benefits of DesignWare PHY IP for TSMC N7+ process including for DDR4, LPDDR, MIPI D-PHY, SD/eMMC, and Multi-Protocol 32G PHYs. Any statements that are not statements of historical fact may be deemed to be forward-looking statements. These statements involve known and unknown risks, uncertainties and other factors that could cause actual results, time frames or achievements to differ materially from those expressed or implied in the forward-looking statements. Such risks and uncertainties include, among others, product timeline and development schedules, or interoperability, performance, and power issues. Other risks and uncertainties that may apply are set forth in the "Risk Factors" section of Synopsys' most recently filed Quarterly Report on Form 10-Q. Synopsys undertakes no obligation to update publicly any forward-looking statements, or to update the reasons actual results could differ materially from those anticipated in these forward-looking statements, even if new information becomes available in the future.

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