

# Synopsys Design Platform Enabled for TSMC's Multi-die 3D-IC Advanced Packaging Technologies

TSMC and Synopsys Collaboration Delivers Design Flow for TSMC's WoW and CoWoS Packaging Technologies

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## Highlights:

- Synopsys Design Platform enabled for TSMC's WoW direct stacking and CoWoS technologies
- Solution includes multi-die and interposer layout implementation as well as parasitic extraction and timing analysis coupled with physical verification
- Reference flow enables early customers to realize the full potential of 3D-IC for high-performance and low-power applications

Synopsys, Inc. (Nasdaq: SNPS) today announced the Synopsys Design Platform fully supports TSMC's wafer-on-wafer (WoW) direct stacking and chip-on-wafer-on-substrate (CoWoS<sup>®</sup>) advanced packaging technologies. The design platform enablement, combined with the 3D-IC reference flow, enables customer deployments for high-performance, high-connectivity multi-die technology in mobile computing, network communication, consumer, and automotive electronics applications.

The platform-wide Synopsys solution includes multi-die and interposer layout capture, physical floorplanning, and implementation, as well as parasitic extraction and timing analysis coupled with physical verification. Key products and features of the Synopsys Design Platform supporting TSMC's advanced WoW and CoWoS packaging technologies include:

- **IC Compiler<sup>™</sup> II place-and-route:** Supports multi-die floorplanning and implementation, including interposer and 3D stack-die generation, TSV placement and connectivity assignment, orthogonal multi-layer, 45-degree single-layer, and interface inter-die block generation for inter-die extraction and checking
- **StarRC<sup>™</sup> extraction:** Supports modeling of TSV and backside RDL metal extraction, silicon interposer extraction, and inter-die coupling capacitance extraction
- **IC Validator:** Supports full-system DRC and LVS verification, inter-die DRC, and LVS checking of inter-die interface
- **PrimeTime<sup>®</sup> signoff analysis:** Full-system static timing analysis, supports multi-die static timing analysis (STA)

"High-performance advanced 3D silicon fabrication and wafer stacking technologies require new EDA features and flows to support the corresponding increase in design and verification complexity," said Suk Lee, TSMC senior director, Design Infrastructure Marketing Division. "We extend our collaboration with Synopsys to deliver design solutions for TSMC's CoWoS and WoW advanced packaging technologies. We look forward to our mutual customers benefiting from the enabled design solutions, boosting designer productivity and accelerating time-to-market."

"Built through deep collaboration, the design solution and reference flow for TSMC's WoW and CoWoS chip integration solutions will enable our mutual customers to achieve optimal quality of results," said Michael Jackson, corporate vice president of marketing and business development for Synopsys' Design Group. "The Synopsys Design Platform and methodologies will allow designers to confidently meet their

schedules for cost-effective, high-performance, and low-power multi-die solutions."

Synopsys jointly highlighted the advances and collaborations of TSMC 2.5D and 3D technologies in a paper titled "Onwards and Upwards: How Xilinx is Leveraging TSMC's Latest Integration and Packaging Technologies with Synopsys' Platform-wide Solution for Next-generation Designs" at the TSMC Open Innovation Platform<sup>®</sup> (OIP) Ecosystem Forum on October 3, 2018 in Santa Clara, California.

### **About Synopsys**

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software<sup>™</sup> partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15<sup>th</sup> largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP, and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at [www.synopsys.com](http://www.synopsys.com).

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