Synopsys Digital and Custom Design Platforms Certified on TSMC 5-nm EUV-based Process Technology

Certification Delivers Proven Production-ready Flow for Advanced Customer Designs

MOUNTAIN VIEW, Calif., Oct. 1, 2018 /PRNewswire/ --

Highlights:

- IC Compiler II and Design Compiler Graphical offer a unified flow to deliver optimized power, performance, and area
- StarRC, PrimeTime, and PrimeTime PX enable full-flow implementation and signoff support for timing and power analysis
- Synopsys Custom Platform with advanced simulation solution supports new 5-nm design rules and FinFET device models

Synopsys, Inc. (Nasdaq: SNPS) today announced that TSMC has certified both the Synopsys Digital and Custom Design Platforms for the latest version of its most advanced, extreme-ultra-violate (EUV)-based, 5-nanometer (nm) process technology. This certification is the result of an extensive, multi-year collaboration to deliver an optimized design solution that speeds the path to next-generation designs.

The Design Compiler® Graphical synthesis tool underwent rigorous 5-nm enablement validation and has demonstrated correlated timing, area, power, and congestion to IC Compiler™ II place-and-route. Design Compiler Graphical 5-nm capabilities deliver improved performance, power, and area driven by new technology innovations, including enhancements to via-pillar optimization, multibit banking, and pin-access optimization.

Key to delivering the required design density are enhancements in IC Compiler II to handle complex, multi-variant and two-dimensional cell placement natively during optimization while maximizing downstream routability and overall design convergence.

Parametric on-chip variation (POCV) analysis in Synopsys' PrimeTime® timing analysis and signoff solution has been enhanced to accurately capture increased non-linear variation due to process scaling and low-voltage operations commonly used to achieve energy efficiency. In addition, PrimeTime physically-aware ECO is expanded to support more complex layout rules for improved congestion, placement, and pin access awareness.

"This 5-nanometer, EUV-enabled node is a core milestone for TSMC and continues to extend our leadership in the broader industry for best-in-class process technology offerings," said Suk Lee, TSMC senior director, Design Infrastructure Marketing Division. "We have worked closely with Synopsys on flow simplification and accelerated time-to-results to enable mutual customers to adopt this new process node using the Synopsys Design Platform. This collaboration has maximized process entitlement for high-performance computing and ultra-low power mobile applications, and we look forward to continuing this for our next-generation node."

"Early path-finding and extensive collaboration with TSMC has enabled mutual customers to take full advantage of the TSMC 5-nanometer process technology using the Synopsys Design Platform," said Michael Jackson, corporate vice president of Marketing at Synopsys. "Our joint commitment to this effort has accelerated customer access to the 5-nanometer process node, speeding the world's highest-density designs to production with best-in-class power, performance, and area."

Synopsys Design Platform technology files, libraries, and parasitic data are available from TSMC for the 5-nm technology process. Key products and features of the Synopsys Design Platform certified by TSMC for its 5-nm FinFET process include:

- **IC Compiler II place-and-route:** Fully automated, full-color routing and extraction support, next-generation placement and legalization technologies to mitigate cell footprint shrinks, and advanced legalization and pin-access modeling for high design utilization.
- **PrimeTime signoff timing:** Advanced variation modeling for low voltages and enhanced ECO technologies with support for new physical design rules.
- **PrimeTime PX power analysis:** Advanced power modeling to accurately analyze leakage effects of ultra-high-density standard cell designs.
- **StarRC signoff extraction:** Advanced modeling to handle the complexity of 5-nm devices, as well as a common technology file for parasitic extraction consistency from synthesis to place-and-route to signoff.
- **IC Validator physical signoff:** Qualified DRC, LVS, and fill runsets developed natively, and released at the same time that TSMC released the design rules.
- **HSPICE®, CustomSim™, and FineSim® simulation solutions:** FinFET device modeling with Monte Carlo feature

support, and accurate circuit simulation results for analog, logic, high-frequency, and SRAM designs.

- **CustomSim reliability analysis:** Accurate dynamic transistor-level IR/EM analysis for 5-nm EM rules.
- **Custom Compiler™ custom design:** Support for new 5-nm design rules, coloring flow, poly track regions, and new MEOL connectivity requirements.
- **NanoTime custom timing analysis:** Runtime and memory optimization for 5-nm devices, POCV analysis for FinFET stacks, and enhanced signal integrity analysis for custom logic, macros, and embedded SRAMs.
- **ESP-CV custom functional verification:** Transistor-level symbolic equivalence checking for SRAM, macros, and library cell designs.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

Editorial Contact:
James Watts
Synopsys, Inc.
650-584-1625
jwatts@synopsys.com

SOURCE Synopsys, Inc.