Graphcore Uses Synopsys Design Platform to Implement Colossus Chip to Accelerate AI Computing

Synopsys Fusion Technology Enables Superior Power, Performance, Area for AI Chip Design

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Highlights:

- Comprehensive Synopsys digital and custom design flows, enhanced with key AI-focused optimization technologies, deliver best-in-class QoR and TTR
- Graphcore selected Synopsys Design Platform with Fusion Technology for its superior power, performance, and area results, and faster design closure
- Synopsys successfully enables massively parallel, graph-centric SoC comprised of 23.5+ billion transistors and 1200+ floating-point processors

Synopsys, Inc. (Nasdaq: SNPS) today announced that Graphcore has used the Synopsys Design Platform to successfully implement its Colossus™ intelligent processing unit (IPU) to accelerate artificial intelligence (AI) computing compared to existing processors (CPUs and GPUs). Comprehensive Synopsys digital and custom design flows, enhanced with key AI-focused optimization technologies, enable designers to achieve target quality-of-results (QoR) and time-to-results (TTR) goals on their AI chips for cloud computing, data center, automotive, and mobile applications. Synopsys' Fusion Technology™ has been augmented with optimization capabilities for AI chip design, including interconnect planning, multiply-accumulate (MAC) topology optimization, and complete AI IP reference flows for maximum speed, smallest area, lowest power, or an optimum balance of the three.

The demand for AI processing potency has been doubling every 3.5 months since 2012 (source: OpenAI), however, the escalating performance, power, and latency required to achieve the processing level are pushing the limits of existing CPU and GPU processors. Graphcore's Colossus IPU is optimized for AI workloads, and can hold entire neural networks on the chip. It employs graph computing with massively parallel, low-precision floating-point compute, and provides much higher compute density than other solutions to accelerate both training and inference for machine learning.

"The Synopsys Design Platform with Fusion Technology provides all of the capabilities we need to achieve superior processing performance for artificial intelligence and machine learning," said Phil Horsfield, vice president of Silicon at Graphcore. "Our partnership with Synopsys has been instrumental in developing the Colossus IPU in a fast-moving, dynamic market for driving current and future AI applications."

The typical AI chip consists of thousands of replicated processor cores, characterized by high throughput, energy efficiency, and low latency. The processor core is the critical building block, with challenging connectivity requirements that can lead to routability-limiting congestion. Synopsys Fusion Technology is the preferred choice for AI chips, providing the best power, performance, congestion/area, yield, and design closure. It has been enhanced with several key AI-focused optimization technologies, including AI chip interconnect planning for hundreds of replicated modules, MAC topology optimization, complete AI IP reference flows, full-flow concurrent clock and data optimization, wire synthesis, and logic restructuring. Comprehensive digital and custom design flows comprised of Design Compiler® Graphical synthesis, IC Compiler™ II place-and-route, PrimeTime® signoff, StarRC® extraction, Custom Compiler® custom layout, SiliconSmart® characterization, and HSPICE® circuit simulation deliver best-in-class QoR and TTR.

"As a leader in AI chip design, Synopsys has been working with pioneers in computer vision, object and speech recognition, and big data analytics," said Sassine Ghazi, co-general manager, Design Group at Synopsys. "Graphcore's Colossus IPU is a major achievement in machine learning, empowering AI applications to move data across the chip orders-of-magnitude more efficiently, while significantly reducing any wasted processing power. Synopsys' Fusion Technology is enabling AI chip companies like Graphcore to quickly bring to market highly-differentiated, industry-defining Super Chips with Synopsys."

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

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