Synopsys Delivers 10X Performance in Formal Property Verification with Breakthrough Machine Learning Technology

VC Formal Regression Mode Accelerator Enables Successively Faster Formal Convergence

MOUNTAIN VIEW, Calif., Aug. 27, 2018 /PRNewswire/ -- Synopsys, Inc. (NASDAQ: SNPS), today announced a state-of-the-art artificial intelligence (AI) enabled formal verification app, Regression Mode Accelerator, as part of the Synopsys VC Formal® solution. This VC Formal app leverages state-of-the-art machine learning algorithms to deliver 10X speed-up in formal property verification during the design and verification cycle. Along with significant performance speed-up, use of this app accelerates formal property verification to achieve better convergence of formal proofs for subsequent runs. The Regression Mode Accelerator app also allows for significant saving of compute resources in nightly regressions for the verification of complex system-on-chip (SoC) designs to enable running formal verification in situations previously deemed impractical.

"As a leading integrated device manufacturer delivering solutions that are key to innovation and advancing the state-of-the-art in Smart Driving and the Internet of Things, including Smart Industry, ST's designers need a formal verification solution that provides best-in-class performance, ease-of-use, and quality of results," said David Vincenzoni, R&D Design Manager at STMicroelectronics. "The newly introduced VC Formal Regression Mode Accelerator app consistently delivered an order-of-magnitude performance improvement along with improved convergence of additional inconclusive properties for the most complex SystemVerilog Assertions on our design blocks."

Increasing SoC complexity combined with rising time-to-market pressures are driving a continuous need for innovation in formal property verification performance and throughput. Synopsys VC Formal, with its comprehensive set of formal apps, including Property Verification (FPV), Sequential Equivalence Checks (SEQ), Register Verification (FRV), Formal Coverage Analyzer (FCA), Connectivity Checking (CC) and Automatic Extraction of Properties (AEP), has delivered faster property convergence for many different use cases at ST. The native integration of VC Formal with Synopsys' VCS® functional verification solution and Verdi® automated debug system enables design and verification teams to easily leverage formal technologies and automate root-cause analysis of formal results. Additionally, the native integration of VCS' robust coverage engines in VC Formal facilitates easy insertion of formal analysis into the existing verification environment.

"Machine-learning has emerged as a powerful technology for addressing the verification of highly-complex and leading-edge designs," said Manish Pandey, Synopsys Fellow in the Verification Group. "We have long collaborated with industry leaders like ST on the delivery of comprehensive verification solutions for advanced SoCs. Throughout these collaborations, we are broadening our investment in AI-enabled technologies into verification flows and methodologies, enabling faster time-to-market."

Availability

The 2018.09 release of VC Formal with Regression Mode Accelerator is scheduled to be available in September 2018.

Additional Resources

For more information on VC Formal please visit:
InFormal Chat blog: https://blogs.synopsys.com/informal-chat/
VC Formal webpage: www.synopsys.com/vcformal

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

Forward-Looking Statements

This press release contains forward-looking statements within the meaning of Section 21E of the Securities Exchange Act of 1934, including statements regarding the expected release and benefits of the 2018.09 release of VC Formal with Regression Mode Accelerator. Any statements that are not statements of historical fact may be deemed to be forward-looking statements. These statements involve known and unknown risks, uncertainties and other factors that could cause actual results, time

frames or achievements to differ materially from those expressed or implied in the forward-looking statements. Such risks and uncertainties include, among others, a customer's specific use cases, or the complexity of various SoC designs. Other risks and uncertainties that may apply are set forth in the "Risk Factors" section of Synopsys' most recently filed Quarterly Report on Form 10-Q. Synopsys undertakes no obligation to update publicly any forward-looking statements, or to update the reasons actual results could differ materially from those anticipated in these forward-looking statements, even if new information becomes available in the future.

Editorial Contact:

James Watts
Synopsys, Inc.
650-584-1625
jwatts@synopsys.com

SOURCE Synopsys, Inc.