# IBM and Synopsys Accelerate Post-FinFET Process Development with DTCO Innovations

Synopsys Manufacturing, IP, and Design Implementation Technologies Enable Industry's Only Complete DTCO Flow

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**Highlights:**

- DTCO methodology reduces cost and time-to-market in advanced semiconductor process development using Synopsys' Sentaurus, Process Explorer, StarRC, SiliconSmart, PrimeTime, and IC Compiler II
- Synopsys' accurate materials, lithography, process, and device TCAD simulators enable evaluation of process options before wafers are available
- Concurrent standard-cell library and block-level design with IC Compiler II enables the use of design-level metrics to select materials, transistor architectures, and process options to meet power, performance, area, and cost (PPAC) targets

Synopsys, Inc. (Nasdaq: SNPS) today announced a collaboration with IBM to apply design technology co-optimization (DTCO) to the pathfinding of new semiconductor process technologies for post-FinFET technologies. DTCO is a methodology for efficiently evaluating and down-selecting new transistor architectures, materials and other process technology innovations using design metrics, starting with an early pathfinding phase before wafers become available. The collaboration will extend the current Synopsys DTCO tool flow to new transistor architectures and other technology options while enabling IBM to develop early process design kits (PDKs) for its partners to assess the power, performance, area, and cost (PPAC) benefits at IBM's advanced nodes.

"Process technology development beyond 7 nanometers requires the exploration of new materials and transistor architectures to achieve optimum manufacturability, power, performance, area, and cost. A major challenge for foundries is to converge on the best architecture in a timely manner while vetting all the possible options," said Dr. Mukesh Khare, vice president of Semiconductor Research, IBM Research Lab. "Our DTCO collaboration with Synopsys allows us to efficiently select the best transistor architecture and process options based on metrics derived from typical building blocks, such as CPU cores, thus contributing to faster process development at reduced cost."

In this collaboration, IBM and Synopsys are developing and validating new patterning techniques with Proteus[TM] mask synthesis, modeling new materials with QuantumATK, optimizing new transistor architectures with Sentaurus[TM] TCAD and Process Explorer, and extracting compact models with Mystic. Design rules and process assumptions derived from these process innovations are used to design and characterize a standard cell library while Fusion Technology[TM] at the block level using the Synopsys physical implementation flow based on IC Compiler[TM] II place-and-route, StarRC[TM] extraction, SiliconSmart® characterization, PrimeTime® signoff, and IC Validator physical verification benefits the evaluation of PPAC.

The scope of the joint development agreement covers multiple facets, including:

- DTCO to optimize transistor- and cell-level design across routability, power, timing, and area
- Evaluate and optimize new transistor architectures, including gate-all-around nanowire and nanoslab devices, with process and device simulation
- Optimize variation-aware models for SPICE simulation, parasitic extraction (PEX), library characterization, and static timing analysis (STA) to accurately encapsulate the effects of variation on timing and power for highest-reliability design with least over-design and design flow runtime overhead
- Gather gate-level design metrics to refine the models, library architecture, and design flows to maximize PPAC benefits

"Synopsys has developed the only complete DTCO solution, from materials exploration to block-level physical implementation," said Dr. Antun Domic, chief technology officer at Synopsys. "IBM's extensive process development and design know-how makes them an ideal partner for extending our DTCO solution to post-FinFET technologies."

For more information on DTCO, visit www.synopsys.com/DTCO.

**About Synopsys**

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software[TM] partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership

in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

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