Synopsys Targets 400G Hyperscale Data Centers with High-Performance Ethernet IP

DesignWare 56G Ethernet PHY Addresses the Reach and Performance Requirements of Next-Generation Leaf-Spine Network Architectures

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Highlights:

- New DesignWare 56G Ethernet PHY supporting PAM-4 and NRZ signaling targets 100G, 200G, and 400G Ethernet applications
- Silicon-proven, configurable transmitter and DSP-based receiver with analog-to-digital converters, reduce power consumption and optimize performance
- High-speed PHY supports optical and copper cable, as well as backplane interfaces for top-of-rack switches
- Unique, scalable PHY architecture enables next-generation 112G interfaces for 800G Ethernet applications

Synopsys, Inc. (Nasdaq: SNPS) today announced the new DesignWare® 56G Ethernet PHY IP for emerging 400 gigabit-per-second (Gbps) hyperscale data center system-on-chips (SoCs). The advanced 56G Ethernet PHY architecture incorporates Synopsys' silicon-proven data converters with a configurable transmitter and digital signal processor (DSP)-based receiver to deliver the best power and performance tradeoffs for the target application. To meet the bandwidth needs of leaf-spine architectures, the PHY supports single and aggregated link rates from 10G to 400G Ethernet, while meeting the PAM-4 and NRZ signaling. In addition, the PHY exceeds the performance requirements of OIF and IEEE standards for chip-to-chip, backplane, and copper/optical cable interfaces. The combination of Synopsys' 56G Ethernet PHY, digital controllers, verification IP, and source code test suites gives designers a complete Ethernet IP solution for their networking data center systems.

For a more robust timing recovery and better jitter performance, the 56G Ethernet PHY receiver features a multi-loop clock and data recovery circuit, as well as a full-featured DSP. The unique architecture of the PAM-4 transmitter allows for precise feed forward equalization to achieve channel performance requirements. The 56G Ethernet PHY's scalable architecture provides a foundation for next-generation 800G Ethernet applications requiring 112G connectivity.

"The growing amount of bandwidth required in the data center is increasing the workload demand on the network infrastructure," said John Koeter, vice president of marketing for IP at Synopsys. "Synopsys' DesignWare 56G Ethernet IP allows designers to meet the high-performance Ethernet connectivity requirements of 400G hyperscale data center SoCs with less risk."

Availability & Additional Resources

The silicon design kit for the DesignWare 56G Ethernet PHY in 16-nm and 7-nm FinFET processes are scheduled to be available in Q3 of 2018 and Q4 of 2018, respectively.

For more information, visit the DesignWare 56G Ethernet PHY IP, DesignWare Ethernet IP Solutions, and VC Verification IP for Ethernet web pages.

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes logic libraries, embedded memories, embedded test, analog IP, wired and wireless interface IP, security IP, embedded processors, and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP prototyping kits, IP software development kits, and IP subsystems. Synopsys' extensive investment in IP quality, comprehensive technical support, and robust IP development methodology enable designers to reduce integration risk and accelerate time-to-market. For more information on DesignWare IP, visit https://www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

Forward-Looking Statements

This press release contains forward-looking statements within the meaning of Section 21E of the Securities Exchange Act of 1934, including statements regarding the expected release and benefits of the silicon design kit for the DesignWare 56G Ethernet PHY in 16-nm and 7-nm FinFET processes. Any statements that are not statements of historical fact may be deemed to be forward-looking statements. These statements involve known and unknown risks, uncertainties and other factors that could cause actual results, time frames or achievements to differ materially from those expressed or implied in the forward-looking statements. Other risks and uncertainties that may apply are set forth in the "Risk Factors" section of Synopsys' most recently filed Quarterly Report on Form 10-Q. Synopsys undertakes no obligation to update publicly any forward-looking statements, or to update the reasons actual results could differ materially from those anticipated in these forward-looking statements, even if new information becomes available in the future.

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