Synopsys RedHawk Analysis Fusion Certified for Samsung Foundry's 10LPE, 8LPP, 7LPP Advanced-Node Designs

5X Productivity Gains in Power Integrity Analysis and Fixing within IC Compiler II

MOUNTAIN VIEW, Calif., June 22, 2018 /PRNewswire/ --

Highlights:

- Validated 100% correlation with ANSYS® RedHawk™ IR/EM analysis to ensure signoff accuracy to drive early design decisions for more robust design
- Push-button integration of static and dynamic IR-drop analysis and fixing for easy adoption by IC Compiler™ II place-and-route engineers
- Smart power grid augmentation enables design robustness and QoR closure for Samsung Foundry's advanced process offerings

Synopsys, Inc. (Nasdaq: SNPS) today announced continued momentum in the rollout of RedHawk™ Analysis Fusion technology through certification by Samsung Foundry. Synopsys, in close collaboration with Samsung Electronics Co., Ltd., a world leader in advanced semiconductor technology, validated power integrity checks with RedHawk Analysis Fusion in the areas of static IR-drop, dynamic IR-drop, and electromigration (EM) analysis. The focus was on correlation to industry-standard ANSYS RedHawk™ signoff analysis to ensure that early analysis and power integrity optimization would result in rapid power integrity convergence during final signoff.

"Having our design teams use signoff technology to make decisions earlier in the design flow is key to achieving the best power, performance, and area," said Jaehong Park, senior vice president of ASIC & IP Team at Samsung Electronics. "Using RedHawk Analysis Fusion technology in IC Compiler II has resulted in a 5X productivity boost for place-and-route engineers to identify and repair power grid weaknesses. We look forward to including it in our 7LPP reference design flow, along with new auto-fixing capabilities, to further improve our productivity and design QoR."

Significant productivity improvements were realized through the application of Synopsys Fusion Technology™ in ANSYS RedHawk and IC Compiler II place-and-route solution enabling transparent data transfer between the place-and-route environment and power integrity analysis. The resulting productivity improvements are a result of eliminating scripting files and cumbersome flows which require external manipulation of data.

"Following the official launch of RedHawk Analysis Fusion in February, designers have been able to immediately leverage the design optimization benefits of IC Compiler II with embedded industry-standard ANSYS RedHawk rail analysis," said Michael Jackson, corporate vice president of marketing for the Design Group at Synopsys. "Through our deep collaboration with Samsung, we realized productivity gains through the seamless fusion of RedHawk coupled with IC Compiler II automated optimization and repair."

"Enabling RedHawk Analysis Fusion earlier in physical design flows helps designers achieve faster convergence during signoff and better QoR with ANSYS' industry-standard power integrity and reliability analyses," said John Lee, vice president and general manager at ANSYS. "We are excited about the results customers are realizing and will continue to advance our partnership with Synopsys to enable further innovations."

Synopsys will feature Samsung as one of the speakers at the Fusion Technology RTL-to-GDSII lunch event on June 25, 2018 at the Design Automation Conference (DAC), to share their experience and the benefits derived from using RedHawk Analysis Fusion technology.

About Fusion Technology

Synopsys' breakthrough Fusion Technology transforms the RTL-to-GDSII design flow with the fusion of best-in-class optimization and industry-golden signoff tools, enabling designers to accelerate the delivery of their next-generation designs with the industry-best full-flow quality of results (QoR) and the fastest time-to-results (TTR). It redefines conventional EDA tool boundaries across synthesis, place-and-route, and signoff, sharing engines across the industry's premier digital design tools, and using a unique, fusion data model for both logical and physical representation. Fusion Technology enables a single DNA backbone across the Synopsys Design Platform that includes IC Compiler II place-and-route, Design Compiler® Graphical synthesis, PrimeTime® signoff, StarRC™ extraction, IC Validator physical verification, DFTMAX™ test, TetraMAX® II automatic test pattern generation (ATPG), SpyGlass® DFT ADV RTL testability analysis, and Formality® equivalence checking. It provides Design Fusion, ECO Fusion, Signoff Fusion, and Test Fusion, resulting in the most predictable RTL-to-GDSII flow with the fewest iterations, as well as unsurpassed design frequency, power, and area.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

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