Synopsys Custom Design Platform Accelerates Robust Custom Design for Samsung Foundry's 7LPP Process Technology

Samsung and Synopsys Release 7LPP Custom Design Reference Flow

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Highlights:

- Synopsys' Custom Design Platform is ready for Samsung Foundry's 7LPP process with certified tools, PDK, simulation models, runsets, and a custom reference flow
- Synopsys Custom Compiler™ layout, HSPICE® simulation, FineSim® SPICE simulation, CustomSim™ FastSPICE simulation, StarRC™ parasitic extraction, and IC Validator physical signoff tools have been certified for Samsung 7LPP design
- Custom design reference flow for Samsung Foundry 7LPP with Synopsys tools includes tutorials on simulation, Monte Carlo analysis, visually-assisted layout automation, parasitic analysis, and electromigration

Synopsys, Inc. (Nasdaq: SNPS) today announced that Samsung Electronics Co., Ltd., a world leader in advanced semiconductor technology, has certified the Synopsys Custom Design Platform for Samsung Foundry's 7-nanometer (nm) Low Power Plus (LPP) process Samsung Foundry's 7LPP is its first semiconductor process technology to use extreme ultraviolet (EUV) lithography, a state-of-the-art process technology that greatly reduces complexity and offers significantly better yield and fast turnaround time when compared to its 10-nanometer (10nm) FinFET predecessors. Synopsys custom design tools have been updated to support Samsung Foundry's 7LPP requirements. In addition, a Synopsys-ready process design kit (PDK) and custom design reference flow are available from Samsung Foundry.

The Synopsys Custom Design Platform has been certified for Samsung Foundry's 7LPP process technology. The platform is centered around the Custom Compiler custom design and layout environment, and includes HSPICE, FineSim SPICE and CustomSim FastSPICE circuit simulation, StarRC parasitic extraction, and IC Validator physical verification. To support efficient 7LPP custom design, Synopsys and Samsung Foundry have collaborated to develop a reference flow that includes a set of tutorials illustrating key requirements of 7-nm design and layout. These tutorials include sample design data and step-by-step instructions for performing typical design and layout tasks. Topics covered include electrical rule checking, circuit simulation, mixed-signal simulation, Monte Carlo analysis, layout, parasitic analysis, and electromigration.

To achieve certification from Samsung Foundry, Synopsys tools have been optimized to support the demanding requirements of 7-nm design, including:

- Accurate FinFET device modeling with device aging effect
- Advanced Monte Carlo simulation features to enable efficient analysis
- High-performance transient noise simulation for analog and RF designs
- High-performance post-layout simulation to enable parasitic-aware design and simulation
- Dynamic circuit ERC for device voltage checks
- High-performance transistor-level EM/IR analysis to minimize over-design
- Efficient symbolic editing of FinFET device arrays
- EUV support
- Coverage-based via resistance extraction

"Our custom design collaboration with Synopsys has expanded substantially over the past two years," said Ryan Sanghyun Lee, vice president of Foundry Marketing Team at Samsung Electronics. "With this latest effort, we have added Synopsys Custom Design Platform support for our 7LPP process, including a custom design reference flow based on Synopsys tools."

"We've been collaborating closely with Samsung Foundry to simplify custom design using FinFET process technology," said Bijan Kiani, vice president of product marketing at Synopsys. "Together we have delivered certified tools, a reference flow, a PDK, simulation models, and runsets to enable Samsung customers to achieve robust custom designs on the 7LPP process."

About Synopsys Custom Design Platform

The Synopsys Custom Design Platform is a unified suite of design and verification tools that accelerates the

development of robust custom designs. Anchored by the Custom Compiler custom design environment, the platform features industry-leading circuit simulation performance and a fast, easy-to-use custom layout editor. It includes technologies for parasitic extraction, reliability analysis, and physical verification.

Key capabilities of the platform include physically-aware design, visually-assisted layout, reliability-aware verification, and IC Compiler™ II co-design. Physically-aware design minimizes the mismatch between pre- and post-layout simulation by fusing technologies from StarRC parasitic extraction into simulation and layout. Visually-assisted layout provides automation without requiring complicated constraints. Reliability-aware verification ensures robust design with signoff-accurate transistor-level EM/IR analysis, large-scale Monte Carlo simulation, aging analysis, and other verification checks. IC Compiler II co-design connects Synopsys' digital and analog tools to into a combined solution for mixed-signal system-on-chip (SoC) implementation. The Synopsys Custom Design Platform is based on the OpenAccess database, includes open APIs for third-party tool integration, and supports programming in TCL and Python. Platform tools include HSPICE and FineSim SPICE, CustomSim FastSPICE, Custom Compiler layout and schematic editor, StarRC parasitic extraction, and IC Validator physical verification. For more information, visit www.customcompiler.info.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

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