Vatics Standardizes on Synopsys' Fusion Technology for its Next-Generation Multimedia SoC Design

Fusion Technology Delivers 40% Runtime Reduction on a 6-million-instance Complex Multi-Voltage Chip

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Highlights:

- Fusion Technology enables Vatics to achieve highest design performance while eliminating ECO iterations on their 28-nm multimedia SoC design
- ECO Fusion delivers signoff accuracy during optimization to drive highest performance, smallest die size, and lowest power
- Synopsys' Fusion Technology combines the best-in-class implementation solution with industry-golden signoff analysis engines, delivering best design QoR and fastest TTR

Synopsys, Inc. (Nasdaq: SNPS) today announced that Vatics, Inc., a trusted leader in advanced multimedia technologies, has adopted Synopsys' Fusion Technology™ for its next-generation multimedia system-on-chip (SoC) design. The result of a close collaboration between the two companies has enabled Fusion Technology to be used successfully to accelerate design closure on advanced low-power multimedia designs at Vatics. Fusion Technology transforms the RTL-to-GDSII design flow with the fusion of best-in-class optimization and industry-golden signoff tools, enabling designers to accelerate the delivery of their next-generation designs with industry-best full-flow quality-of-results (QoR) and the fastest time-to-results (TTR). It redefines conventional EDA tool boundaries across synthesis, place-and-route, and signoff, sharing engines across the industry's premier digital design tools and using a unique Fusion data model for both logical and physical representation.

"At Vatics, we are designing some of the most complex image processing SoCs where meeting design cycle times and market window are essential to our success," said Shor Shen, CEO of Vatics. "We have collaborated with Synopsys to validate ECO Fusion technology on a very complex 28-nanometer, 6-million-instance, high-performance, multi-voltage design, and significantly reduced our design closure time by 40 percent. Pursuant to this successful experience, we are widely deploying ECO Fusion technology on all our production designs and feel confident that Synopsys' groundbreaking Fusion Technology will expedite delivery of our products to market."

Fusion Technology enables sharing of technologies across tool boundaries with Design Fusion, ECO Fusion, Signoff Fusion, and Test Fusion. Design Fusion provides best QoR and fast convergence with common engines between synthesis and place-and-route, which allows technologies to move seamlessly between synthesis and place-and-route. ECO Fusion drives faster signoff closure based on PrimeTime® static timing analysis and StarRC™ extraction signoff engines. ECO Fusion technologies, such as exhaustive path-based analysis, eliminate ECO iterations and deliver signoff design closure for implementation design scenarios. ECO Fusion also includes PrimeTime's new machine learning technology that delivers significant speed-up for ECO power recovery without compromising timing QoR. Signoff Fusion uses the golden signoff backbone for both optimization and signoff to enable perfect correlation, reduced pessimism, and superior QoR. Test Fusion is the combination of design-for-test RTL analysis and design-for-test synthesis integrated into implementation, enabling best QoR and reducing silicon test costs.

"We created Fusion Technology to improve designer productivity and deliver best design QoR for leading market segments where hitting market windows is business-critical," said Michael Jackson, corporate vice president of marketing and business development for Synopsys' Design Group. "By fusing our market-leading products, Fusion Technology offers unprecedented full-flow productivity and better power, performance, and area design metrics. Vatics' deployment of ECO Fusion capabilities is a testament to the power of our cutting-edge Fusion Technology."

To learn more about how Fusion Technology is enabling designers to accelerate their next generation designs, attend the Synopsys Fusion Technology RTL-to-GDSII lunch event on June 25, 2018 at the Design Automation Conference (DAC). To register for this event visit https://www.synopsys.com/company/resources/events/dac2018/events/fusion.html.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

Editorial Contact:
James Watts
Synopsys, Inc.
650-584-1625
jwatts@synopsys.com

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