Synopsys' Latest ARC MetaWare EV Development Toolkit Release Speeds Application Software Development for Embedded Vision Systems

Enhanced Tools Reduce Computation, Memory, and Bandwidth Requirements for Mapping Neural Network Graphs to DesignWare EV6x Vision Processor IP

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Highlights:

- DesignWare ARC MetaWare EV Development Toolkit provides a comprehensive and integrated software programming environment for Synopsys' EV6x Embedded Vision Processors based on the latest vision standards
- New ARC MetaWare EV release automatically maps neural network graphs to EV6x with new options that reduce computational, memory, and bandwidth requirements
- Optimized kernels and runtime environment conforming to the latest OpenVX 1.2 specification simplify development of embedded vision application code

Synopsys, Inc. (Nasdaq: SNPS), today announced a new release of its DesignWare® ARC® MetaWare EV Development Toolkit, an integrated programming environment that accelerates application software development for the DesignWare ARC EV6x family of embedded vision processors. The latest release of the ARC MetaWare EV Development Toolkit includes a range of enhancements for improving programmer productivity, including reduced computational, memory, and bandwidth requirements for mapping convolutional neural network (CNN) graphs to the EV6x's heterogeneous processing elements without compromising graph accuracy. The Toolkit supports both Caffe and Tensorflow deep-learning frameworks and CNN graphs trained with 8-bit or 12-bit precision. The latest tool release also includes advanced graph compression and runtime feature map compression/decompression capabilities to increase performance and lower power consumption.

The ARC MetaWare EV Development Toolkit offers a programming environment for the EV6x vision processor IP based on the OpenVX™ open standard API, with a C/C++ compiler and OpenCL™ C vectorizing compiler. The Toolkit includes OpenVX kernels optimized to run on EV6x Processors, the first hardware-software platform to successfully pass The Khronos Group's OpenVX 1.2 conformance tests. The OpenVX framework simplifies the programming of the EV6x processors by automatically distributing kernel execution over the EV6x's scalar, vector, and CNN engine units. The OpenCL C compiler offers automatic whole function vectorization, which exploits data-level parallelism by transforming scalar kernels into SIMD instructions that compute on the processor's vector DSPs. The MetaWare EV compiler supports all the programmability of the 512-bit wide vector DSP.

For early application development, the Toolkit provides an instruction set simulator for the EV6x processor family. In addition, the included Virtualizer Development Kit (VDK) provides a system-level virtual prototype consisting of a host processor connected to the EV6x processor with a functional CNN engine simulation model. This enables early application development in the context of a more complete system, and the full suite of tools and libraries enables programmers to efficiently build, debug, profile, and optimize their embedded vision systems.

"High productivity development tools are a fundamental requirement of embedded vision application design, requiring advanced tools and software that conform to industry standards to accelerate this effort," said John Koeter, vice president of marketing for IP at Synopsys. "The latest enhancements to the ARC MetaWare EV Development Toolkit provides embedded vision developers with a complete and integrated toolset that addresses key requirements of embedded vision applications, including the main CNN frameworks, enabling them to get their DesignWare ARC EV6x Processor-based products to market faster."

Availability

The 2018.06 release of the ARC MetaWare EV Development Toolkit for DesignWare ARC EV6x Vision Processors for both Windows and Linux workstations is scheduled to be available in June 2018.

Learn more about Synopsys' MetaWare EV Development Toolkit
Learn more about Synopsys' DesignWare EV6x Processor Family

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio

includes logic libraries, embedded memories, embedded test, analog IP, wired and wireless interface IP, security IP, embedded processors and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP prototyping kits, IP software development kits and IP subsystems. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enables designers to reduce integration risk and accelerate time-to-market. For more information on DesignWare IP, visit http://www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

Forward-Looking Statements

This press release contains forward-looking statements within the meaning of Section 21E of the Securities Exchange Act of 1934, including statements regarding the expected release and benefits of the 2018.06 release of the ARC MetaWare EV Development Toolkit for DesignWare ARC EV6x Vision Processors for both Windows and Linux workstations. Any statements that are not statements of historical fact may be deemed to be forward-looking statements. These statements involve known and unknown risks, uncertainties and other factors that could cause actual results, time frames or achievements to differ materially from those expressed or implied in the forward-looking statements. Other risks and uncertainties that may apply are set forth in the "Risk Factors" section of Synopsys' most recently filed Quarterly Report on Form 10-Q. Synopsys undertakes no obligation to update publicly any forward-looking statements, or to update the reasons actual results could differ materially from those anticipated in these forward-looking statements, even if new information becomes available in the future.

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