TSMC Certifies Synopsys Design Platform for High-performance 7-nm FinFET Plus Technology

Synopsys Design Platform Delivers High-performance, High-density Designs

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Highlights:

- Synopsys Design Platform is certified by TSMC for 7-nm FinFET Plus process technology, with customer deployment on multiple designs
- IC Compiler II optimized for EUV lithography-aware 7-nm FinFET Plus process delivers area savings
- Platform-wide support for multi-die integration using TSMC's Wafer-on-Wafer® (WoW) technology improves productivity and time-to-volume

Synopsys, Inc. (Nasdaq: SNPS) today announced certification of the Synopsys Design Platform with TSMC's latest Design Rule Manual (DRM) for advanced 7-nanometer (nm) FinFET Plus process technology. With several test chips taped out and production designs currently under development by multiple customers, this certification by TSMC enables a wide range of designs from high-performance computing and high-density to low-power mobile applications using the Synopsys Design Platform.

This certification is a milestone for TSMC's extreme ultraviolet lithography (EUV) process that enables significant area savings while maintaining high performance when compared to non-EUV process nodes.

The Synopsys Design Platform, anchored by Design Compiler® Graphical synthesis and IC Compiler™ II place-and-route tools, has been enhanced to take full advantage of TSMC's 7-nm FinFET Plus for high-performance designs. Design Compiler Graphical is capable of automatically inserting via pillar structures to boost performance and prevent signal electromigration (EM) violations, and can pass the information to IC Compiler II for further optimization. It also automatically applies non-default rules (NDR) during synthesis and performs layer-aware optimization to improve design performance. These optimizations, including IC Compiler II bus routing, continue throughout the place-and-route flow to meet stringent delay-matching requirements of high-speed network.

PrimeTime® timing analysis advanced waveform propagation (AWP) and parametric on-chip variation (POCV) technologies have been optimized to address increased waveform distortion and non-Gaussian variation effects of higher performance and lower voltage operation. In addition, PrimeTime's physically-aware signoff has been expanded to support via-pillars.

Synopsys has enhanced the Design Platform to perform physical implementation, parasitic extraction, physical verification, and timing analysis to support TSMC's WoW technology. The physical implementation flow with IC Compiler II provides full support for wafer staking designs, from initial die floorplan preparation to placement and assignment of bumps to implementation of die routing. Verification is done by IC Validator for DRC/LVS checks, and Synopsys' StarRC™ tool performs parasitic extraction.

"Ongoing collaboration with Synopsys and early customer engagements on TSMC's 7-nanometer FinFET Plus process technology are delivering differentiated platform solutions that help our mutual customers bring innovative new products to market faster," said Suk Lee, senior director of the Design Infrastructure Marketing Division at TSMC. "Certification of the Synopsys Design Platform enables our mutual customers' designs in our first mass-production, EUV-enabled technology."

"Our collaboration with TSMC on their mass-production 7-nanometer FinFET Plus process allows companies to confidently begin designing their increasingly large SoC and multi-die chips with the highly-differentiated Synopsys Design Platform," said Michael Jackson, corporate vice president of marketing and business development for the Design Group at Synopsys. "Certification on TSMC's 7-nanometer FinFET Plus process enables our customers to benefit from significant power, performance, and area improvements of an advanced EUV process, while accelerating time-to-market for their differentiated products."

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors,

or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

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