Synopsys and TSMC Collaborate to Deliver DesignWare Foundation IP for Ultra-Low Power TSMC 22-nm Processes

DesignWare Logic Library, Embedded Memory and OTP NVM IP for TSMC 22ULP and 22ULL Processes Improves Power Consumption for Digital Home, IoT, and Mobile Devices

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Highlights

- DesignWare Duet Packages for TSMC 22ULP and 22ULL processes provide all of the memory and logic libraries needed to implement a complete SoC
- DesignWare HPC Design Kit for the TSMC 22ULP process delivers improved performance, power, and area for CPU, GPU, and DSP processor cores
- DesignWare OTP NVM IP for TSMC 22ULP and 22ULL processes supports up to 1Mb instances without additional mask layers or process steps for applications such as calibration, encryption keys, and secure code storage
- STAR Memory System embedded test, repair, and diagnostics solution improves test quality with minimal impact on timing and area

Synopsys, Inc. (Nasdaq: SNPS) today announced its collaboration with TSMC to develop DesignWare® Foundation IP for TSMC's 22-nanometer (nm) ultra-low power (ULP) and ultra-low leakage (ULL) processes. DesignWare Foundation IP, including logic libraries, embedded memories, and one-time programmable (OTP) non-volatile memories (NVM) on TSMC's 22-nm processes, enables designers to significantly reduce power consumption while meeting performance requirements for a wide range of applications. The DesignWare Duet Packages of Foundation IP include high-speed, area-optimized, and low-power embedded memories, logic libraries built with either standard core oxide or thick IO oxide for ultra-low leakage, STAR Memory System® memory test and repair capabilities, and power optimization kits to provide the highest quality of results for an SoC. The DesignWare HPC Design Kit, a suite of high-speed and high-density memory instances and logic cells, enables SoC designers to optimize their CPU, GPU, and DSP cores for an optimum balance of speed, area, and power. The DesignWare OTP NVM IP for TSMC's 22ULP and 22ULL processes does not require additional mask layers or process steps and provides high yields, security, and reliability in a small footprint.

"TSMC and Synopsys share a long track record of successful collaboration to help our mutual customers achieve their SoC performance, power, and area targets," said Suk Lee, senior director of the Design Infrastructure Marketing Division at TSMC. "By offering DesignWare Foundation IP for TSMC's 22ULP and 22ULL processes, Synopsys continues to be a leading provider of proven IP solutions that enable designers to reduce design effort and achieve their design goals on TSMC's latest process technologies."

"Synopsys and TSMC have worked closely through many generations of TSMC process technologies to provide high-quality foundation IP that helps designers meet the power, performance, and area requirements of their SoCs," said John Koeter, vice president of marketing at Synopsys. "Synopsys' DesignWare Logic Library and Embedded Memory IP for TSMC's 22ULP and 22ULL processes enable designers to dramatically reduce power consumption for their target applications and bring differentiated products to market faster."

Availability

The DesignWare Duet Packages for TSMC's 22ULP and 22ULL processes and HPC Design Kits for TSMC's 22ULP process are scheduled to be available in Q3 2018. The DesignWare OTP NVM IP is scheduled to be available for 22ULP in Q3 2018, and for 22ULL in Q1 2019.

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes logic libraries, embedded memories, embedded test, analog IP, wired and wireless interface IP, security IP, embedded processors and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP prototyping kits, IP software development kits and IP subsystems. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enable designers to reduce integration risk and accelerate time-to-market. For more information on DesignWare IP, visit www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the

electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

Forward-Looking Statements

This press release contains forward-looking statements within the meaning of Section 21E of the Securities Exchange Act of 1934, including statements regarding the expected release and benefits of the DesignWare Duet Packages and OTP NVM for TSMC's 22ULP and 22ULL processes and HPC Design Kit for TSMC's 22ULP process. Any statements that are not statements of historical fact may be deemed to be forward-looking statements. These statements involve known and unknown risks, uncertainties and other factors that could cause actual results, time frames or achievements to differ materially from those expressed or implied in the forward-looking statements. Other risks and uncertainties that may apply are set forth in the "Risk Factors" section of Synopsys' most recently filed Quarterly Report on Form 10-Q. Synopsys undertakes no obligation to update publicly any forward-looking statements, or to update the reasons actual results could differ materially from those anticipated in these forward-looking statements, even if new information becomes available in the future.

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