Synopsys Digital and Custom Design Platform Certified for TSMC's Most Advanced 5-nm Process Technology for Early Design Starts

Close Collaboration Enables Designers to Benefit from the Process' Power, Performance, and Area for the Most Advanced Designs

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Highlights:

- IC Compiler II optimized to enable low power with high design utilization for TSMC's latest 5-nm process technology, maximizing the benefits of this new node
- Advanced enablement across the full Synopsys Design Platform supports advanced modeling of low-voltage operation
- Enhanced circuit simulation modeling for 5-nm FinFET devices in HSPICE, CustomSim, and FineSim, and support for new layout rules in Custom Compiler

Synopsys, Inc. (Nasdaq: SNPS) today announced the certification of its Synopsys Design Platform for early design starts on TSMC's latest version of its most advanced 5-nanometer (nm) process technology. Enabled through close and early collaboration with TSMC, the IC Compiler™ II place-and-route solution deploys next-generation placement and legalization technologies to co-maximize routability and overall design utilization. Leveraging significant design technology co-optimization work, support for highly-compact cell libraries is additionally enabled through implementation in IC Compiler II with ECO closure that utilizes PrimeTime® signoff and StarRC™ extraction technologies. For TSMC's 5-nm extreme ultraviolet lithography (EUV) process, new opportunities for parasitic optimization are additionally maximized through deployment of common technologies for non-default rule handling and layer optimization, resulting in a highly-convergent RTL-to-GDSII implementation solution.

Advanced technologies in the PrimeTime timing analysis and signoff solution are extended throughout the digital implementation platform to enable differentiated designs in high-growth markets targeting TSMC's 5-nm process node. Parametric on-chip variation (POCV) analysis in PrimeTime was enhanced to accurately capture increased non-linear variation due to process scaling and low-voltage operations commonly used to achieve energy efficiency in the targeted applications as noted above.

TSMC 5-nm certification also includes IC Validator physical signoff, with support for DRC, LVS and metal fill. The runsets are released at the same time when TSMC releases the design rules. Deep technology collaboration between TSMC and Synopsys enables advanced process features such as new poly mesh fill enhancements and LVS dual-hierarchy extraction.

To accelerate robust custom and analog/mixed-signal (AMS) design, the HSPICE® simulation, and CustomSim™ and FineSim® FastSPICE simulators have been enhanced to support TSMC's 5-nm FinFET process. Combined with CustomSim advanced IR/EM reliability analysis capabilities, this solution accelerates AMS verification to enable robust AMS design.

"Collaborating with Synopsys on 5-nanometer enablement supports customers to design at low voltage while maintaining high performance," said Suk Lee, senior director of the Design Infrastructure Marketing Division at TSMC. "To help customers achieve target PPA with our 5-nanometer process technology, TSMC and Synopsys have worked together on a broad range of design styles to push and maximize the design performance."

"Given the complexity of rules and advances in the 5-nanometer process technology, we had to further shift-left the start of collaboration cycle with TSMC," said Michael Jackson, corporate vice president of marketing and business development for the Design Group at Synopsys. "In addition, we also had to shift-left our engagement with the early adopters of 5-nanometer technology. New nodes are getting introduced at an unprecedented pace, and our collaboration with TSMC ensures that companies can confidently design at the new nodes while maximizing returns from their investment."

Synopsys Design Platform technology files, libraries, and parasitic data are available from TSMC for early design starts on the 5-nm technology process. Key products and features of the Synopsys Design Platform certified by TSMC for its 5-nm FinFET process include:

- IC Compiler II place-and-route: Fully automated, full-color routing and extraction support, next-generation placement and legalization technologies to mitigate cell footprint shrinks, advanced legalization and pin-access modeling for high design utilization, and a full-flow deployment of via-pillar technology to concurrently maximize performance and device yield.
- PrimeTime signoff timing: Advanced modeling for low voltages.
- StarRC signoff extraction: Advanced modeling for FinFET device extension.
- IC Validator physical signoff: DRC, LVS, and fill runsets developed concurrently, and DRC runset was released at the

same time that TSMC released the design rules.
- HSPICE, CustomSim and FineSim simulation solutions: FinFET device modeling with Monte Carlo feature support; accurate circuit simulation results for analog, logic, high-frequency, and SRAM designs.
- Custom Compiler™ custom design: Support for TSMC 5-nm new design rules.
- NanoTime custom timing analysis: Advanced transition-based POCV variation analysis and enhanced signal integrity analysis with optimized aggressor handling for embedded SRAMs and custom macros.
- ESP custom functional verification: Transistor-level symbolic equivalence checking for SRAM, macros, and library cell designs.
- CustomSim reliability analysis: accurate dynamic transistor-level IR/EM analysis for advanced EM rules support.

About Synopsys

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