

# Synopsys Introduces Breakthrough Fusion Technology to Transform the RTL-to-GDSII Flow

Fusion of Best-in-Class Optimization and Industry-golden Signoff Tools Delivers Best Full-flow Quality-of-Results and Fastest Time-to-Results

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## Highlights:

- Fusion Technology redefines conventional design tool boundaries, sharing engines across the industry's premier digital design tools, and using a unique, Fusion data model for both logical and physical representation
- Design Fusion, ECO Fusion, Signoff Fusion, and Test Fusion enable the most predictable RTL-to-GDSII flow with the fewest iterations
- Fusion Technology enables SoC designers to achieve unsurpassed design frequency, power, and area

Synopsys, Inc. (Nasdaq: SNPS) today unveiled its breakthrough Fusion Technology that transforms the RTL-to-GDSII design flow with the fusion of best-in-class optimization and industry-golden signoff tools, enabling designers to accelerate the delivery of their next-generation designs with industry-best full-flow quality-of-results (QoR) and the fastest time-to-results (TTR). It redefines conventional EDA tool boundaries across synthesis, place-and-route and signoff, sharing engines across the industry's premier digital design tools, and using a unique, Fusion data model for both logical and physical representation.

Fusion Technology enables one DNA backbone across the Synopsys Design Platform that includes IC Compiler™ II place-and-route, Design Compiler® Graphical synthesis, PrimeTime® signoff, StarRC™ extraction, IC Validator physical verification, DFTMAX™ test, TetraMAX® II automatic test pattern generation (ATPG), SpyGlass® DFT ADV RTL testability analysis, and Formality® equivalence checking solutions. It provides Design Fusion, ECO Fusion, Signoff Fusion, and Test Fusion, resulting in the most predictable RTL-to-GDSII flow with the fewest iterations, as well as unsurpassed design frequency, power, and area.

"Collaborating with Synopsys on Fusion Technology is enhancing our ability to serve customers in the fields of machine learning, high-performance computing, and automotive," said Jaehong Park, senior vice president, ASIC & IP Team at Samsung Electronics. "We have experienced 10 percent better QoR using Design Fusion, and ECO turnaround time of less than one day by using ECO Fusion, along with the seamless integration of ANSYS® RedHawk™ software, on our most challenging advanced-node designs. We believe Synopsys' Fusion Technology is a game-changing innovation in the semiconductor industry, and it will certainly help Samsung Foundry, as well as our customers, to bring innovative products to market more quickly."

The traditional RTL-to-GDSII design flow has clear lines of demarcation between synthesis, place-and-route, and signoff functions. These functional boundaries cause rework when transitioning from one design phase to the next, as the less-precise engines used early in the flow are replaced by more-precise engines closer to tapeout. Design iterations at the transition point between tools lead to degraded full-flow TTR and unmet power, performance, and area (PPA) targets.

Fusion Technology redefines conventional EDA tool boundaries and enables Design Fusion, ECO Fusion, Signoff Fusion, and Test Fusion. Design Fusion provides common engines between synthesis and place-

and-route to enable convergence, and moves synthesis optimization technology into place-and-route, and place-and-route optimization technology into synthesis in order to enable best QoR. ECO Fusion drives faster signoff closure based on PrimeTime and StarRC golden signoff analysis inside implementation, improving flow predictability and eliminating ECO iterations. Signoff Fusion eliminates excessive design margin and overdesign, using the golden signoff backbone for both optimization and signoff, to enable perfect correlation, reduced pessimism, and superior QoR. Test Fusion is the combination of design-for-test RTL analysis and design-for-test synthesis integrated into implementation, enabling best QoR while reducing silicon test costs and turnaround time.

"Semiconductor industry shifts are straining the traditional RTL-to-GDSII flow, particularly at the EDA tool functional boundaries which manifest non-linear, non-monotonic, non-convergent discontinuities, leading to design iterations," said Sassine Ghazi, co-general manager and corporate staff, Design Group at Synopsys. "Fusion Technology was developed to improve the full-flow productivity of RTL-to-GDSII design teams, by fusing together our best-in-class optimization and industry-golden signoff analysis. It is gratifying to see promising results and reactions from our customers, who are experiencing fewer design iterations, eliminating ECO loops, and exceeding their chip design QoR and schedule targets."

Learn more about Fusion Technology and the unique Design Fusion, ECO Fusion, Signoff Fusion, and Test Fusion capabilities in our [whitepaper](#).

Early-adoption customers and our exclusive rail analysis partner, ANSYS, will discuss their experiences and results using Fusion Technology at the [Synopsys Users Group](#) (SNUG®) Silicon Valley event, March 21-22, at the Santa Clara Convention Center in Santa Clara, Calif.

### **About Synopsys**

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15<sup>th</sup> largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at <http://www.synopsys.com/>.

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