Synopsys Enables Robust Design Optimization for Next-generation High-performance Computing, Mobile and Automotive Products with IC Compiler II and RedHawk Analysis Fusion

First Product Available from Exclusive Partnership with ANSYS that Brings Power Integrity and Reliability Signoff Technology Earlier in the Design Flow

MOUNTAIN VIEW, Calif., March 19, 2018 /PRNewswire/ --

Highlights:

- Production capability delivered on schedule per partnership announcement inJune 2017
- Analysis/optimization of voltage drop and electromigration reduces ECOs and cycle time
- Seamless integration enhances ease-of-use with virtually no learning curve
- Up to 5X turnaround time improvement vs. point tool power integrity fixing flows

Synopsys, Inc. (Nasdaq: SNPS), in collaboration with ANSYS, today announced the immediate availability of RedHawk™ Analysis Fusion, a complete in-design power integrity add-on solution for Synopsys IC Compiler™ II place-and-route system users. Synopsys brings to production a fully integrated rail analysis flow that leverages IC Compiler II's best in-class power, performance, and area (PPA) with industry-standard RedHawk rail analysis from ANSYS. RedHawk Analysis Fusion enables place-and-route engineers to perform early power grid integrity checks, as well as static and dynamic power analysis at multiple points in the design flow and from within the familiar IC Compiler II cockpit.

Productivity gains are maximized by collapsing numerous steps associated with point tool flows into a single command. Seamless visualization of IR drop maps from within the IC Compiler II environment also means faster issue debug, which reduces ECO cycle time. Designers can expect true convergence without unexpected violations during final power signoff analysis, because the underlying results are generated by the same ANSYS® RedHawk™ power analysis engine.

"With our close partnership and collaboration with ANSYS, we were able to successfully roll out our RedHawk Analysis Fusion capability on schedule. Designers can immediately leverage the design optimization benefits of IC Compiler II with embedded industry standard ANSYS RedHawk rail analysis," said Michael Jackson, corporate vice president of marketing for the Design Group at Synopsys. "Our customers are especially pleased with the productivity gains achieved by utilizing a single environment that provides seamless execution and visualization of RedHawk analyses coupled with IC Compiler II automated optimization and repair."

"RedHawk Analysis Fusion complements ANSYS' industry-standard power integrity and reliability analyses, and enables designers to unlock better PPA," said John Lee, vice president and general manager at ANSYS. "This partnership empowers new innovations, and we are thrilled with the results customers are already seeing."

Synopsys will feature Toshiba Electronic Devices & Storage Corp. as one of the speakers at the Fusion Technology™ lunch panel at the Synopsys Users Group (SNUG®) Silicon Valley event, March 21-22 at the Santa Clara Convention Center, to discuss their experience and benefits derived from using RedHawk Analysis Fusion.

About Fusion Technology

Synopsys' breakthrough Fusion Technology transforms the RTL-to-GDSII design flow with the fusion of best-in-class optimization and industry-golden signoff tools, enabling designers to accelerate the delivery of their next-generation designs with the industry-best full-flow quality-of-results (QoR) and the fastest time-to-results (TTR). It redefines conventional EDA tool boundaries across synthesis, place-and-route and signoff, sharing engines across the industry's premier digital design tools, and using a unique, single data model for both logical and physical representation. Fusion Technology enables one DNA backbone across the Synopsys Design Platform that includes IC Compiler II, Design Compiler® Graphical synthesis, PrimeTime® signoff, StarRC™ extraction, IC Validator physical verification, DFTMAX™ test, TetraMAX® II automatic test pattern generation (ATPG), SpyGlass® DFT ADV RTL testability analysis, and Formality® equivalence checking. It provides Design Fusion, ECO Fusion, Signoff Fusion, and Test Fusion, resulting in the most predictable RTL-to-GDSII flow with the fewest iterations, as well as unsurpassed design frequency, power, and area.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

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