Synopsys Advances Custom Platform to Accelerate Robust Custom Design

Latest Product Releases Deliver 2X Simulation Speed-up for FinFET and Automotive Designs

MOUNTAIN VIEW, Calif., March 12, 2018 /PRNewswire/ --

Release Highlights:

- 2X FineSim SPICE speed-up for FinFET and Monte Carlo Analysis
- 2X CustomSim speed-up for FinFET SRAMs
- Extended Custom Compiler visually-assisted flow with hand-crafted quality device routing

Synopsys, Inc. (Nasdaq: SNPS) today announced release of the latest versions of its circuit simulation and custom design products—HSPICE®, FineSim® SPICE, and CustomSim simulators and the Custom Compiler™ IC design tool—to address the growing need for robust custom design. The growth in automotive electronics and transition to FinFET process nodes have led to a significant increase in IC design complexity and the need for rigorous analysis to validate custom and analog/mixed-signal (AMS) designs across a broad spectrum of process corners and environmental conditions. The latest releases of Synopsys' custom design solution provide 2X faster simulation and Monte Carlo analysis speed, as well as enhancements to Custom Compiler, including interactive device-level routing to accelerate robust custom design.

Circuit Simulation Performance for Robust Design Validation

FinFET designs have significantly more post-layout parasitics, making transistor-level simulation of large analog and custom digital designs a formidable challenge. The 2017.12 release of FineSim SPICE delivers core engine innovations and RC optimizations to provide 2X speed-up for FinFET post-layout simulation of large designs.

To accelerate robust design validation, the latest release of FineSim SPICE also delivers 2X Monte Carlo simulation speed-up by streamlining Monte Carlo model generation and results post-processing. Similarly, new RC reduction and partitioning algorithms in the 2017.12 release of the CustomSim FastSPICE tool deliver 2X speed-up for post-layout SRAM simulation and maintain multi-core scalability by providing additional 2X speed-up on four cores. Additionally, the 2017.12 release of HSPICE delivers 1.5X speed-up for large post-layout designs.

Custom Compiler Enhancements Accelerate Custom Layout

Custom Compiler's industry-pioneering visually-assisted layout automation technologies provide a substantial boost to custom layout productivity, especially for FinFET process nodes. In the 2017.12 release, this feature set has been enhanced to include device-level pattern routing. Unlike typical routers, the pattern router in Custom Compiler creates connections that mimic interconnect patterns that a layout designer creates by hand. Achieving hand-crafted-quality routes is important for device-level connections, especially for sensitive analog circuitry.

Custom Compiler includes a library of built-in routing patterns. In addition, the pattern router can extract patterns from a hand-created layout and reapply those patterns to other connections that need to be routed. This new feature complements the previously released feature that enables placement patterns in the design to be reused. Now Custom Compiler can place and route devices automatically, following patterns learned from an example layout. We call this approach template-based design, a powerful way to accelerate custom layout by reusing layout knowledge.

"High-reliability applications, such as automotive and FinFET process node designs, pose new challenges for companies needing to ensure custom design robustness," said Bijan Kiani, vice president of marketing at Synopsys. "The latest enhancements in Synopsys' Custom Design Platform enable design teams to accelerate custom and AMS design and validation through innovations in visually-assisted layout automation and simulation performance technologies."

About Synopsys Custom Design Platform

The Synopsys Custom Design Platform is a unified suite of design and verification tools that accelerate the development of robust custom designs. Anchored by the Custom Compiler custom design environment, the Platform features industry-leading circuit simulation performance and a fast, easy-to-use custom layout editor. It includes technologies for parasitic extraction, reliability analysis and physical verification.

Key capabilities of the Platform include physically-aware design, visually-assisted layout, reliability-aware

verification, and IC Compiler™ II co-design. Physically-aware design minimizes the mismatch between pre- and post-layout simulation by fusing technologies from StarRC™ parasitic extraction into simulation and layout. Visually-assisted layout provides automation without requiring complicated constraints. Reliability-aware verification ensures robust design with signoff-accurate transistor-level EM/IR analysis, large-scale Monte Carlo simulation, aging analysis, and other verification checks. IC Compiler II co-design connects Synopsys' digital and analog tools to into a combined solution for mixed-signal system-on-chip (SoC)implementation. The Synopsys Custom Design Platform is based on the OpenAccess database, includes open APIs for third-party tool integration, and supports programming in TCL and Python. Platform tools include HSPICE, FineSim SPICE, and CustomSim FastSPICE simulators, Custom Compiler layout and schematic editor, StarRC parasitic extraction, and IC Validator physical verification. For more information, visit www.customcompiler.info.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

Editorial Contact:
Janet Berkman
Synopsys, Inc.
T: 650-584-5707
jberkman@synopsys.com

SOURCE Synopsys, Inc.