Synopsys Collaborates with Samsung Foundry to Develop DesignWare IP for Samsung 8-nm FinFET Process

Collaboration Provides Lowest-Risk Path to Silicon Success for Designers Developing SoCs in Samsung Processes Targeting Low-Power, High-Performance Applications

MOUNTAIN VIEW, Calif., March 8, 2018 /PRNewswire/ --

Highlights:

- DesignWare Foundation IP, including logic libraries and embedded memories, will deliver superior performance, power, and area on Samsung 8LPP process technology
- ASIL D Ready DesignWare Foundation IP designed to meet automotive Grade 1 temperature (-40C to +150C junction) requirements will accelerate ISO 26262 functional safety assessments and improve automotive SoC reliability
- Collaboration builds on more than 10 years of success, resulting in billions of devices shipped with DesignWare IP on Samsung processes

Synopsys, Inc. (Nasdaq:SNPS) today announced a collaboration with Samsung Foundry to develop DesignWare® Foundation IP for Samsung's 8-nanometer (nm) Low Power Plus (8LPP) FinFET process technology. Providing DesignWare Logic Library and Embedded Memory IP on Samsung's latest process technology enables designers to take advantage of a reduction in power and area compared to Samsung's 10LPP process. The DesignWare Foundation IP will be developed to meet strict automotive-grade requirements, enabling designers to accelerate ISO 26262 and AEC-Q100 qualifications of their advanced driver assistance system (ADAS) and infotainment system-on-chips (SoCs). The DesignWare Logic Library and Embedded Memory IP will be available from Synopsys through the Foundry-Sponsored IP Program for the Samsung 8LPP process, enabling qualified customers to license the IP at no cost. The collaboration extends Synopsys' and Samsung's long history of working together to provide silicon-proven IP that helps designers meet their performance, power, and area requirements for a wide range of applications including mobile, automotive, and cloud computing.

"Samsung's collaboration with Synopsys over the last decade has enabled first-pass silicon success for billions of ICs in mobile and consumer applications," said Jongwook Kye, vice president of Design Enablement at Samsung Electronics. "As designs get more complex and migrate to smaller FinFET processes, Samsung's advanced 8LPP process with Synopsys' high-quality Foundation IP solutions will enable designers to differentiate their products for mobile, cryptocurrency and network/server applications, accelerate project schedules, and quickly ramp into volume production."

"Samsung and Synopsys share a long and successful history of providing designers with silicon-proven DesignWare IP on Samsung's processes ranging from 180 to 10 nanometer," said John Koeter, vice president of marketing for IP at Synopsys. "As the leading provider of physical IP with more than 100 test chip tapeouts on FinFET processes, Synopsys continues to make significant investments in developing IP to help designers take advantage of Samsung's latest process technologies, reduce risk and speed development of their SoCs."

Availability

DesignWare Logic Libraries and Embedded Memories for Samsung 8LPP are scheduled to be available in Q2 2018 at no cost to qualified licensees from Synopsys as part of the Foundry-Sponsored IP Program. Contact Synopsys for details on automotive-grade application support.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

Forward-Looking Statements

This press release contains forward-looking statements within the meaning of Section 21E of the Securities Exchange Act of 1934, including statements regarding the expected release and benefits of the DesignWare IP for Samsung's 8-nm LPP FinFET process technologies. Any statements that are not statements of historical fact may be deemed to be forward-looking statements. These statements involve known and unknown risks, uncertainties and other factors that could cause actual

results, time frames or achievements to differ materially from those expressed or implied in the forward-looking statements. Other risks and uncertainties that may apply are set forth in the "Risk Factors" section of Synopsys' most recently filed Annual Report on Form 10-K. Synopsys undertakes no obligation to update publicly any forward-looking statements, or to update the reasons actual results could differ materially from those anticipated in these forward-looking statements, even if new information becomes available in the future.

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