Synopsys' DesignWare STAR Memory System's New Test and Repair Capabilities Speed Embedded Memory Repair Time by 10x

Enhanced BIST and Repair Algorithms for 7-nm FinFET Processes Increase Memory IP Test Coverage and Accelerate Power-On Initialization

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Highlights:

- Index-based repair capabilities in STAR Memory System cut memory repair cycles from more than 1000 to fewer than 100 cycles by testing only faulty memories
- Enhanced hardware and algorithm support in STAR Memory System detects and corrects 7-nm FinFET-specific fault types
- New self-test and fault injection capabilities within the ECC compiler mitigate soft errors and improve in-field reliability for automotive, mobile and cloud computing SoCs

Synopsys, Inc. (Nasdaq:SNPS) today announced a new suite of embedded memory test and repair features for its DesignWare® STAR Memory System® solution to enable increased test coverage and faster power-on initialization for high-performance automotive, mobile and cloud computing system-on-chips (SoCs). With these new features, designers can achieve a 10x reduction in repair time by eliminating extra cycles and testing only faulty memories. The STAR Memory System includes enhanced hardware and test algorithms to detect and correct a wide variety of dynamic faults prevalent in advanced process technologies, including 7-nm FinFET, both in production test and in the field. In addition, its error correcting code (ECC) compiler mitigates the impact of soft errors by calculating the memory failures in time (FIT) rate, enabling designers to improve the reliability of their systems.

"Moving to a new process node, especially in small geometries, is a big challenge," said Spark Zhang, DFT engineer at HiSilicon. "Using the DesignWare STAR Memory System helped us meet our power, performance, area, and test targets, resulting in first-pass silicon success for our 7-nm FinFET SoC."

"With the increasing amounts of SRAM memory required in today's applications, integrating an efficient test and repair solution can accelerate timing closure and improve system reliability and performance," said John Koeter, vice president of marketing for IP at Synopsys. "The new capabilities in the DesignWare STAR Memory System significantly reduce repair time and improve reliability of SoCs."

Availability & Resources

The STAR Memory System is available now.

- Web site: DesignWare STAR Memory System
- Customer Success: HiSilicon Achieves First-Pass Silicon Success for 7-nm FinFET SoC Using DesignWare Foundation IP

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare® IP portfolio includes logic libraries, embedded memories, embedded test, analog IP, wired and wireless interface IP, security IP, embedded processors and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP prototyping kits, IP software development kits and IP subsystems. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enable designers to reduce integration risk and accelerate time-to-market. For more information on DesignWare IP, visit www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

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