DecaWave Deploys Synopsys TetraMAX II ATPG on Latest Automotive Design to Lower Test Time 50 Percent and Speed Runtime by 10x

Company Standardizes on TetraMAX II Solution to Create Manufacturing Tests for All Designs

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Highlights:

- TetraMAX II ATPG reduced test generation runtime by an order of magnitude, from an overnight run to less than one hour, while producing 50 percent fewer patterns
- DecaWave met their silicon test time budget for their automotive IC using TetraMAX II solution
- DecaWave's adoption of TetraMAX II solution took less than one hour

Synopsys, Inc. (Nasdaq: SNPS) today announced that DecaWave, a manufacturer of low-cost, low-power indoor positioning ICs and modules, deployed TetraMAX® II automatic test pattern generation (ATPG) to significantly reduce runtime from nine hours to thirty minutes and reduce the number of patterns by 50 percent compared to their previous test pattern generation solution for an automotive ultra-wide band transceiver IC. The lower pattern count enabled DecaWave to meet the challenge of high-quality manufacturing testing within a limited amount of tester time. DecaWave incorporated the TetraMAX II solution into their flow with minimal effort and produced improved results within an hour. As a result of this success, DecaWave is standardizing on Synopsys' TetraMAX II solution for all future designs to minimize silicon test costs and maximize test quality.

"Because our automotive IC requires high-quality testing with very few patterns, we decided to try TetraMAX II," said Gavin Marrow, vice president of technology at DecaWave. "TetraMAX II met our stringent requirements, creating 50 percent fewer test patterns compared to our prior ATPG while running 10x faster. Furthermore, we were able to include TetraMAX II in our design flow within only a few minutes and generate patterns immediately. Given the results, we believe TetraMAX II will meet our needs for high test quality across all our designs."

TetraMAX II ATPG is built on new engines that are extremely fast, memory efficient and optimized for generating patterns and diagnosing defect parts. These innovations lead to significantly fewer test patterns and cut runtime from days to hours. The TetraMAX II solution enables use of all server cores regardless of design size, surpassing previous solutions. The ability to reuse production-proven user and tool interfaces ensures designers can quickly and confidently deploy TetraMAX II ATPG on their most challenging designs. The TetraMAX II solution uses established links with Synopsys® Design Platform tools such as DFTMAX™ compression, PrimeTime® timing analysis and StarRC™ extraction as well as other Synopsys tools including Yield Explorer® design-centric yield analysis to deliver the highest quality test and the fastest, most productive flows.

"Synopsys is responding to the need for higher test quality for all of our customers, including those developing automotive ICs, such as DecaWave," said Bijan Kiani, vice president of product marketing at Synopsys. "The success at DecaWave demonstrates the benefits gained from our on-going development of breakthrough technologies, such as those delivered in TetraMAX II ATPG, to meet evolving design and test requirements."

About the Synopsys Synthesis-Based Test Solution

The Synopsys synthesis-based test solution comprises DFTMAX Ultra, DFTMAX, TetraMAX and TetraMAX II technologies for power-aware logic test and physical diagnostics; DFTMAX LogicBIST for in-system self-test; SpyGlass® DFT ADV for testability analysis; the DesignWare® STAR Hierarchical System for automated hierarchical testing of analog/mixed-signal IP, digital logic blocks, memory and interface IP on an SoC; the DesignWare STAR Memory System™ solution for embedded test, repair and diagnostics; the Z01X™ fault simulator; and Yield Explorer design-centric yield analysis. Synopsys' test solution combines Design Compiler® RTL synthesis with embedded test technology to optimize timing, power, area and congestion for test as well as functional logic, leading to faster time-to-results. The Synopsys test solution delivers tight integration across the Synopsys Design Platform, including Design Compiler synthesis, IC Compiler™ II place and route, and PrimeTime timing analysis, to enable faster turnaround time while meeting both design and test goals, higher defect coverage and faster yield ramp.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

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