Synopsys Delivers Industry's First USB 3.2 Verification IP and Test Suite for Higher Performance USB Designs

Native SystemVerilog USB VIP Features Built-in Coverage, Verification Plan, Protocol-Aware Debug and Source Code Test Suites

MOUNTAIN VIEW, Calif., Oct. 5, 2017 /PRNewswire/ -- Synopsys, Inc. (NASDAQ: SNPS) today announced the availability of the industry's first verification IP (VIP) and UVM source code test suite to support the latest USB 3.2 specification. USB 3.2 enables new hosts and devices with USB Type-C™ to be designed as multi-lane solutions, allowing for up to two lanes of 5 Gbps or two lanes of 10 Gbps operation, doubling the data rate over the existing USB Type-C cables. It also supports re-timer enhancements.

"The USB 3.2 specification is an incremental update that defines multi-lane operation for new USB 3.2 hosts and devices with continued use of existing SuperSpeed USB physical layer data rates and encoding techniques," said Jeff Ravencraft, USB-IF president and COO. "Being first in industry, Synopsys VIP for USB 3.2 strengthens the ecosystem and facilitates early adoption and fast development of higher-performance USB designs."

Synopsys VC VIP for USB is based on native SystemVerilog/UVM architecture and features built-in comprehensive coverage, verification plan, extensive protocol checks and integration with Synopsys Verdi® protocol-aware debug for ease of use and increased productivity. Synopsys VIP includes an extensive and customizable set of frame generation, error injection capabilities and comprehensive exception list to generate negative scenarios. In addition, UVM source code test suites are also available to verify features with minimal effort and jumpstart testing of USB designs.

"We continue to collaborate with standard organizations to develop controller, PHY, Verification IP and test suites for the latest protocols and specifications," said Vikas Gautam, group director of VIP R&D and corporate applications for the Synopsys Verification Group. "By delivering USB VIP and test suites, including early support for the latest USB 3.2 standard, Synopsys enables designers to efficiently design the latest USB devices and subsystems and accelerate verification closure."

Availability

Synopsys VC VIP for USB 3.2 and source code test suites are available today to early access customers. Contact Synopsys for more information regarding the DesignWare USB 3.2 controller and PHY IP solution.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

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