Synopsys' IC Compiler II Completes Certification for TSMC's 12-nm Process Technology

Platform-Wide Enhancements Across Digital and Custom Design Tools Deliver a Production-Ready Flow

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Highlights:

- Synopsys Design Platform is certified for TSMC's innovative 12-nm process technology with customer validation on multiple production tape-outs
- PDK availability for the Custom Compiler solution and support for in-design RC extraction, DRC and EM analysis, color-aware interactive routing

Synopsys, Inc. (Nasdaq: SNPS) today announced that TSMC has certified IC Compiler™ II place-and-route system and Synopsys Design Platform for the V1.0 production of its latest 12-nanometer (nm) FinFET process technology. With multiple test-chips completed and production designs already in process, this certification by TSMC paves the way for wide-ranging usage across the broad IC Compiler II and Synopsys Design Platform installed base, enabling mutual customers to derive the maximum benefit of this new technology node.

IC Compiler II design flow has been extensively enhanced, in concert with ECO technologies in the PrimeTime® static timing analysis tool, to support the latest requirements of the 12-nm standard cell and design methodology.

With full flow support for integrating 16-nm IP alongside newer 12-nm higher performing and higher density logic functions, designers are further enabled to draw out the maximum process technology benefits with the highest productivity. Users of Synopsys' IC Validator for physical signoff are now enabled to transition directly to TSMC signoff by utilizing the same decks and methodologies that their 16-nm solutions rely on. IC Validator's double patterning technology (DPT) is enabled, supporting cross-node links between 16-nm and 12-nm technologies, ultimately shortening the time to production tape-out. The 12-nm iPDK includes the PCells and technology data needed for using the Custom Compiler™ layout flow with TSMC's 12-nm process.

"Our latest 12-nm FinFET process helps deliver the return on investment (ROI) benefits associated with 16-nm IP re-use as well as highly differentiated power, performance and area (PPA) benefits," said Suk Lee, TSMC senior director, Design Infrastructure Marketing Division. "We are excited to announce this certification that was delivered in close collaboration with Synopsys and look forward to our mutual customers benefiting from the deployment of this process technology."

"Our collaboration with TSMC on their 12-nm process allows designers to confidently use the highly differentiated Synopsys Design Platform for their increasingly complex chip designs targeting TSMC's cost-effective FinFET process," said Bijan Kiani, vice president of product marketing for the Design Group at Synopsys. "This latest certification further extends a long and deep relationship with TSMC, ensuring that our mutual customers have the maximum opportunity to develop their best-in-class products at any process node."

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP, and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

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