Synopsys IC Compiler II Certified for TSMC's Advanced 7-nm FinFET Plus Node

Platform-Wide Certification for TSMC's Latest Advanced-Process Technology

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Highlights:

- Design Compiler Graphical and IC Compiler II place-and-route validated on multiple 7-nm FinFET Plus high-performance production designs
- PrimeTime and StarRC advanced variation modeling supporting 7-nm FinFET Plus low voltage and high-performance designs with enhanced physically-aware ECO technologies and efficient via pillar modeling
- Support for multi-die integration using TSMC's CoWoS® technology increases productivity and accelerates time to volume

Synopsys, Inc. (Nasdaq: SNPS) today announced that TSMC has certified the Synopsys Design Platform for the latest Design Rule Manual (DRM) of its 7-nm FinFET Plus process technology. Anchored around Synopsys' design implementation solutions of IC Compiler™ II place-and-route system, this certification enables early customer access to TSMC's first mass-market extreme ultraviolet lithography (EUV)-enabled process.

Building on the earlier certification this year for TSMC's 7-nm process technology, the Synopsys Design Platform has been utilized extensively in multiple production tape-outs across wide-ranging market, including high-performance computing (HPC) and mobile.

"With 7-nm FinFET Plus we are doubling down on delivering differentiated platform solutions that help our customers reap the maximum benefit for their broad market or high-value, niche products," said Suk Lee, TSMC senior director, Design Infrastructure Marketing Division. "Our ongoing collaborations with Synopsys have been key in ensuring that we bring extensive value through both productivity and end-market quality-of-results. This work ensures that our mutual customers can maximize return on investment (ROI) as efficiently as possible in their product development cycles."

To further provide differentiation in the expanding mobile and nascent IoT markets, low voltage operation is enabled through PrimeTime® timing analysis technology. Key technologies, such as advanced waveform propagation helps capture advanced node impacts of Miller-capacitances and resistance-centric "long-tail" effects. Parametric on-chip variation (POCV) support, specified through the Liberty™ Variation Format (LVF), has been expanded to capture the non-Gaussian effects at low voltage. Ratified by the Liberty Technology Advisory Board (LTAB), LVF-based POCV is now supported throughout Synopsys' physical implementation and analysis flows, helping mutual customers minimize variation margins with significant quality of results (QoR) improvements in area and total design power. Providing further differentiation for physically-aware signoff is the introduction of via-pillar-aware ECO closure where designers can achieve maximum benefits for performance, yield and total design reliability.

"Our collaboration with TSMC has resulted in multiple successful 7-nm FinFET Plus production designs using the Synopsys Design Platform," said Bijan Kiani, vice president of product marketing for the Design Group at Synopsys. "With the TSMC-certified Synopsys Design Platform, designers can take full advantage of the performance and low power consumption offered by TSMC's advanced technology."

Key products and features of the Synopsys Design Platform certified by TSMC for its 7-nm FinFET Plus process include:

- IC Compiler II place-and-route: full-color routing and extraction, advanced cut-metal modeling for reducing end-of-line spacing, and a full flow deployment of via pillar technology
- PrimeTime signoff timing: advanced variation modeling for low voltage and high-performance designs with enhanced physically-aware ECO technologies
- StarRC™ signoff extraction: process-tuned color-aware variation modeling, efficient via pillar modeling for high-performance designs
- IC Validator physical signoff: certified runsets for signoff DRC and LVS including new multiple patterning rule checks; LVS new extract feature for new/additional parameter for simulation; and 2D expandable FILL enhancements
- HSPICE®, CustomSim™ and FineSim® simulation solutions: FinFET device modeling with self-heating/aging effect and Monte Carlo feature support; accurate circuit simulation results for analog, logic, high-frequency and SRAM designs
- Custom Compiler™ custom design: full coloring interactive routing, DRC checks and density reporting,

color-aware EM and RC reporting
- NanoTime custom timing analysis: advanced analysis of level shifters for low-power designs of embedded SRAMs, and new SRAM precharge and bitline-to-wordline timing checks
- ESP-CV custom functional verification: transistor-level symbolic equivalence checking for SRAM, macros and library cell designs
- CustomSim reliability analysis: accurate dynamic transistor-level IR/EM analysis for self-heat-aware EM rules and advanced via support

With the ever-growing demand for "More-than-Moore" solutions, Synopsys delivers design solutions for TSMC's chip-on-wafer-on-substrate (CoWoS) packaging technology enabling multiple chips side-by-side using a through-silicon-via (TSV)-driven interposer platform. The solutions include IC Compiler II multi-die physical implementation with support for placement, assignment and routing of microbump and TSV; redistribution layer (RDL) and signal routing, and power mesh creation on CoWoS interconnection layers; IC Validator LVS connectivity checking between stacked die and StarRC Ultra parasitic extraction support for TSV, microbump, RDL and signal routing metal with PrimeTime timing analysis of multi-die systems. Comprising analysis, implementation and signoff verification solutions, these latest technologies ensure that mutual customers can extract the maximum ROI for best-in-class, system-level products.

About Synopsys

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