Synopsys Launches Complete HBM2 IP Solution Offering More Than 300 GB/s Bandwidth for Graphics and High-Performance Computing SoCs

New DesignWare HBM2 Controller, PHY and Verification IP Enables High-Bandwidth, Power-Efficient Systems

MOUNTAIN VIEW, Calif., July 25, 2017 /PRNewswire/ --

Highlights:

- Complete HBM2 IP solution, including PHY, controller and verification IP, reduces integration risk while minimizing time-to-market
- DesignWare IP implementation supports data rates up to 2400 Mb/s, which is 20 percent faster than the JEDEC standard specification
- Pseudo-channel mode doubles the number of channels, resulting in smaller fetch size and higher performance
- The HBM2 IP is based on Synopsys' silicon-proven HBM and DDR4 IP that has been integrated into hundreds of SoC designs

Synopsys, Inc. (Nasdaq: SNPS) today introduced its complete DesignWare® High Bandwidth Memory 2 (HBM2) IP solution consisting of controller, PHY and verification IP, enabling designers to achieve up to 307 GB/s aggregate bandwidth, which is 12 times the bandwidth of a DDR4 interface operating at 3200 Mb/s data rate. In addition, the DesignWare HBM2 IP solution delivers approximately ten times better energy efficiency than DDR4. Advanced graphics, high-performance computing (HPC) and networking applications are requiring more memory bandwidth to keep pace with the increasing compute performance brought by advanced process technologies. With the DesignWare HBM2 IP solution, designers can achieve their memory throughput requirements with minimal power consumption and low latency. The new DesignWare HBM2 IP solution is built on Synopsys' silicon-proven HBM and DDR4 IP, which has been validated in hundreds of designs and shipped in millions of systems-on-chips (SoCs), enabling designers to lower integration risk and accelerate adoption of the new standard.

"We selected Synopsys' DesignWare HBM2 IP solution to take full advantage of the bandwidth and power efficiency of the 16GB of HBM2 memory in our Radeon™ Vega Frontier Edition graphics cards," said Joe Macri, corporate VP and product CTO at AMD. "Synopsys' deep expertise in memory interfaces enabled us to successfully integrate HBM2 IP into the 'Vega' GPU architecture and achieve aggressive power and memory bandwidth targets to serve machine learning and advanced graphics applications."

The complete DesignWare HBM2 IP solution provides unique functionality that enables designers to achieve their memory bandwidth, latency and power objectives. The DesignWare HBM2 Controller supports pseudo-channel operation in either lock step or memory interleaved mode, allowing users to maximize bandwidth based on their unique traffic pattern. Both the HBM2 controller and PHY utilize a DFI 4.0-compatible interface to simplify integration with custom DFI-compliant controllers and PHYs.

The DesignWare HBM2 PHY IP offers four trained power management states and fast frequency switching that allows the SoC to manage power consumption by quickly changing between operating frequencies. The DesignWare HBM2 PHY enables a microbump array that matches the JEDEC HBM2 SDRAM standard for the shortest possible 2.5D package routes and highest signal integrity. To simplify HBM2 SDRAM testing, the DesignWare HBM2 PHY IP provides an IEEE 1500 port with an access loopback mode for testing and training the link between the SoC and HBM2 SDRAM.

Synopsys VC Verification IP for HBM is fully compliant to HBM JEDEC specification (including HBM2) and provides protocol, methodology, verification and productivity features including built-in protocol checks, coverage and verification plans, and Verdi® protocol-aware debug and performance analysis, enabling users to achieve rapid verification of HBM-based designs.

"Increasing memory bandwidth without overtaxing power and area budgets is critical for graphics, HPC and networking applications," said John Koeter, vice president of marketing for IP at Synopsys. "As the leading providing of memory IP, Synopsys has engaged closely with several lead customers to develop an HBM2 IP solution that enables designers to address increasing throughput requirements, with improved latency and power efficiency for their high-performance SoC designs."

Availability & Resources

The DesignWare HBM2 PHY and VC Verification IP are available now for 14- and 7-nm process technologies, with additional process technologies in development. For availability information on the DesignWare HBM2 Controller IP, please contact Synopsys.

- Register for the upcoming webinar: DDR4 or HBM2 High Bandwidth Memory: How to Choose Now
- Learn more about DesignWare HBM2 IP
- Learn more about VC Verification IP for HBM2

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes logic libraries, embedded memories, embedded test, analog IP, wired and wireless interface IP, security IP, embedded processors and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP prototyping kits, IP software development kits and IP subsystems. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enables designers to reduce integration risk and accelerate time-to-market. For more information on DesignWare IP, visit www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

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